

1 / 73

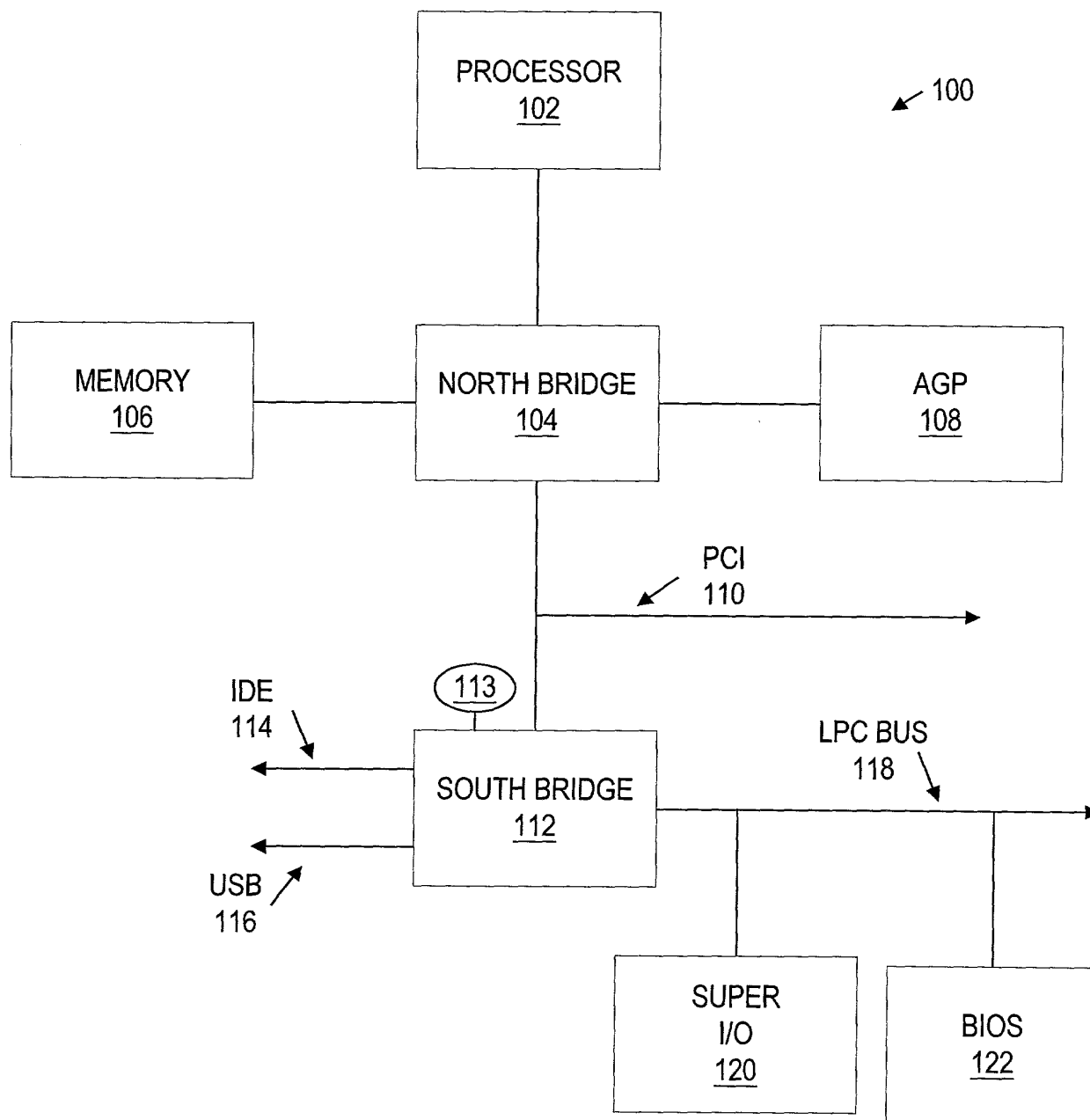


Fig. 1A
(Prior Art)

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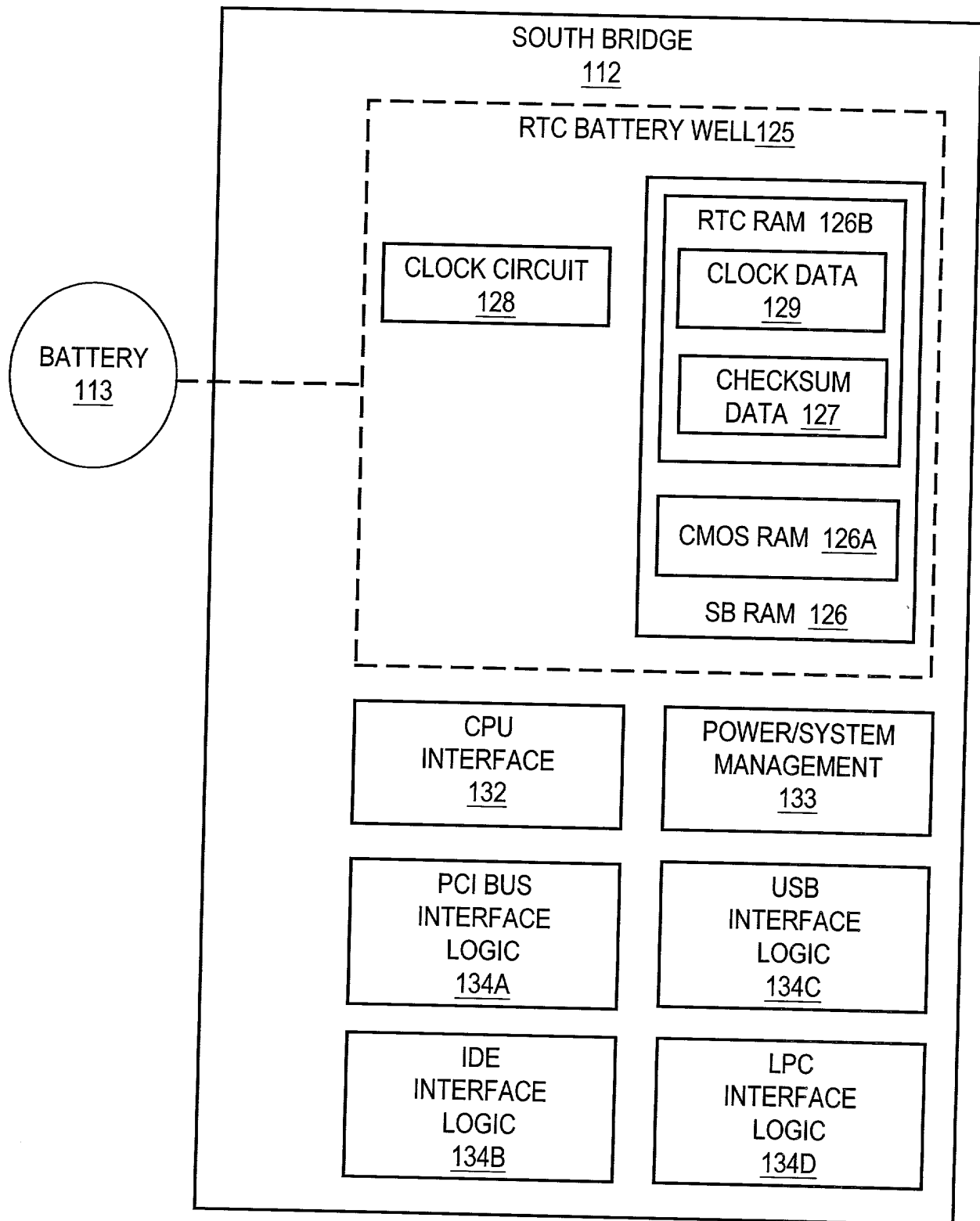


Fig. 1B
(Prior Art)

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135

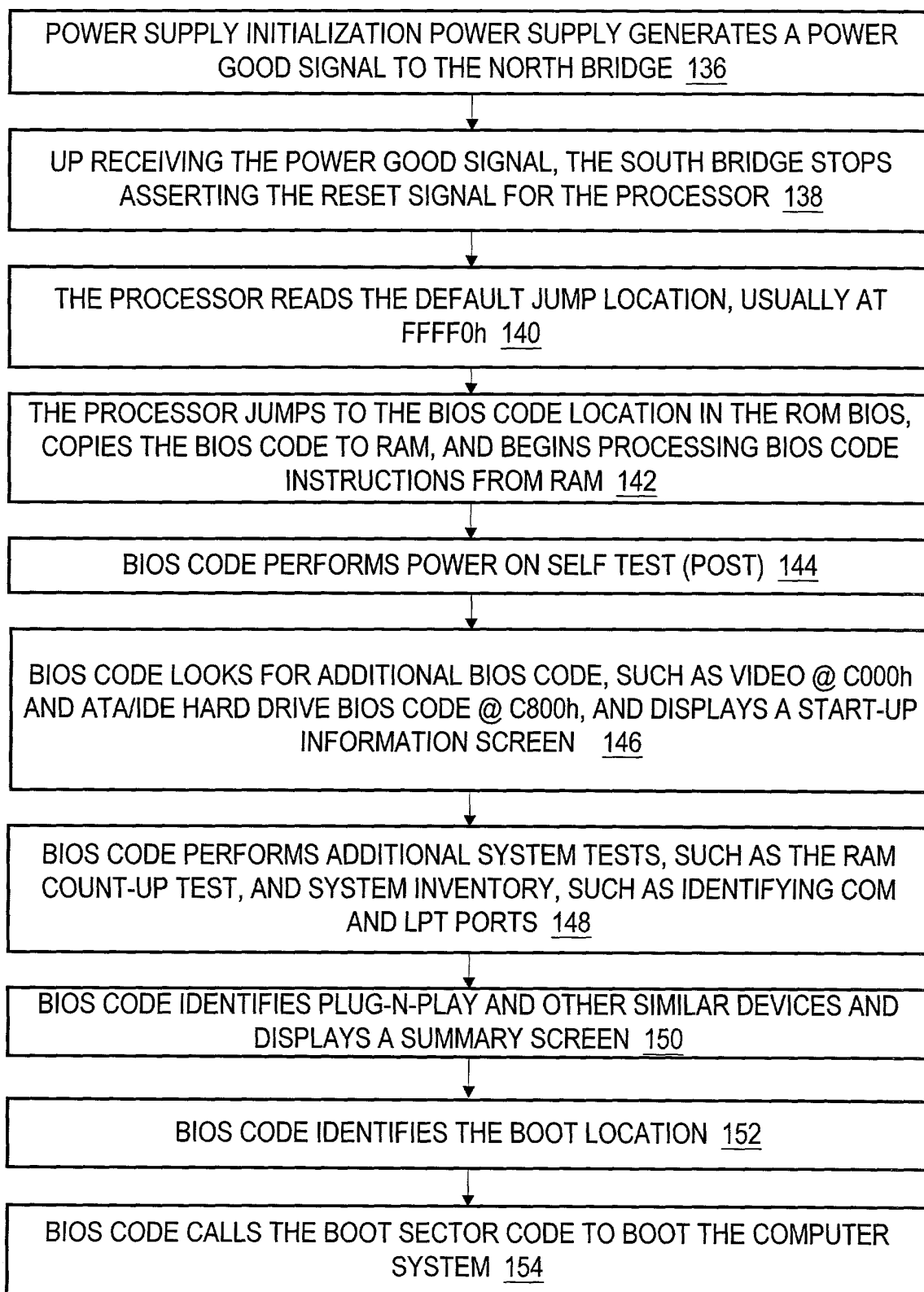


Fig. 2A
(Prior Art)

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170

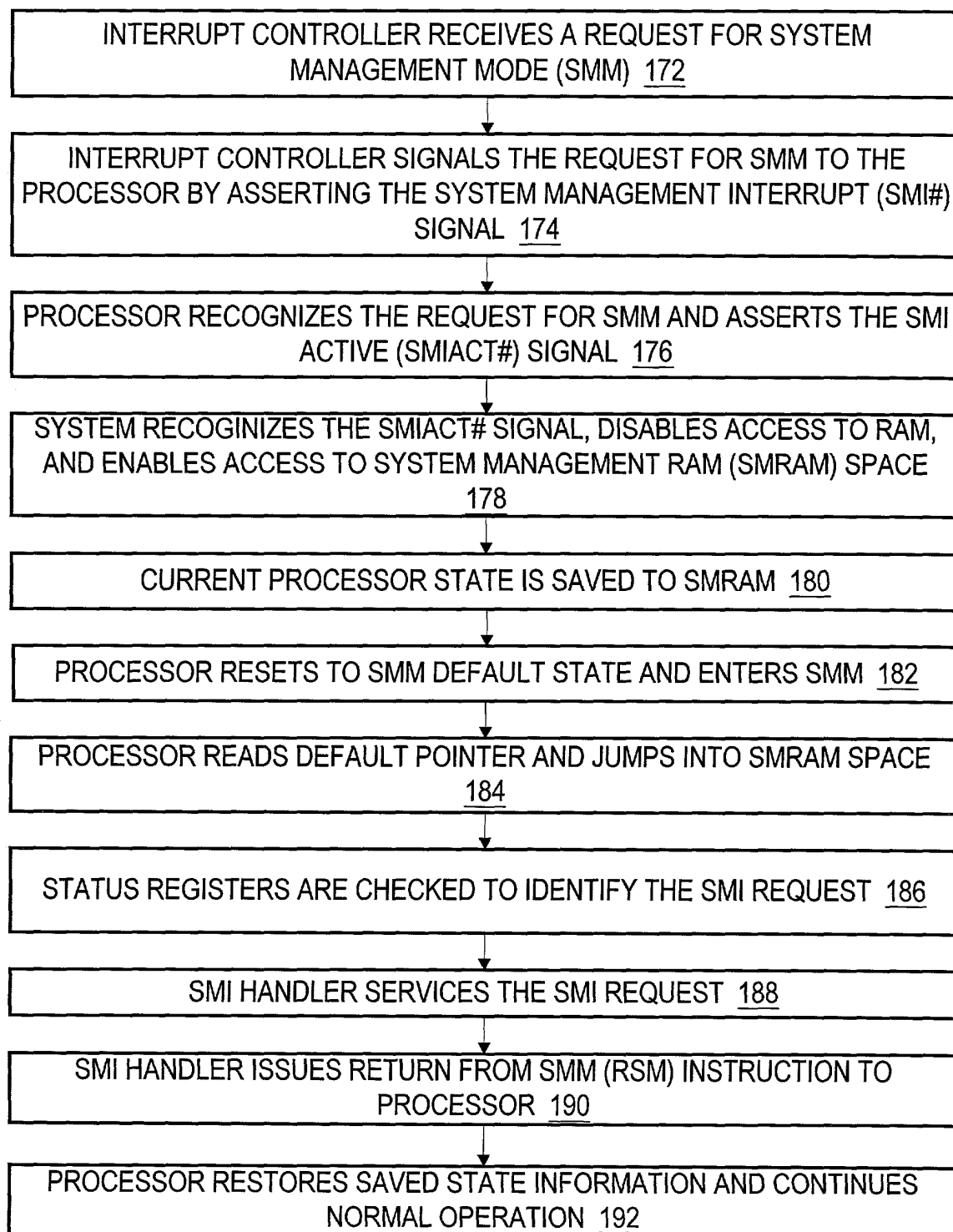


Fig. 2B
(Prior Art)

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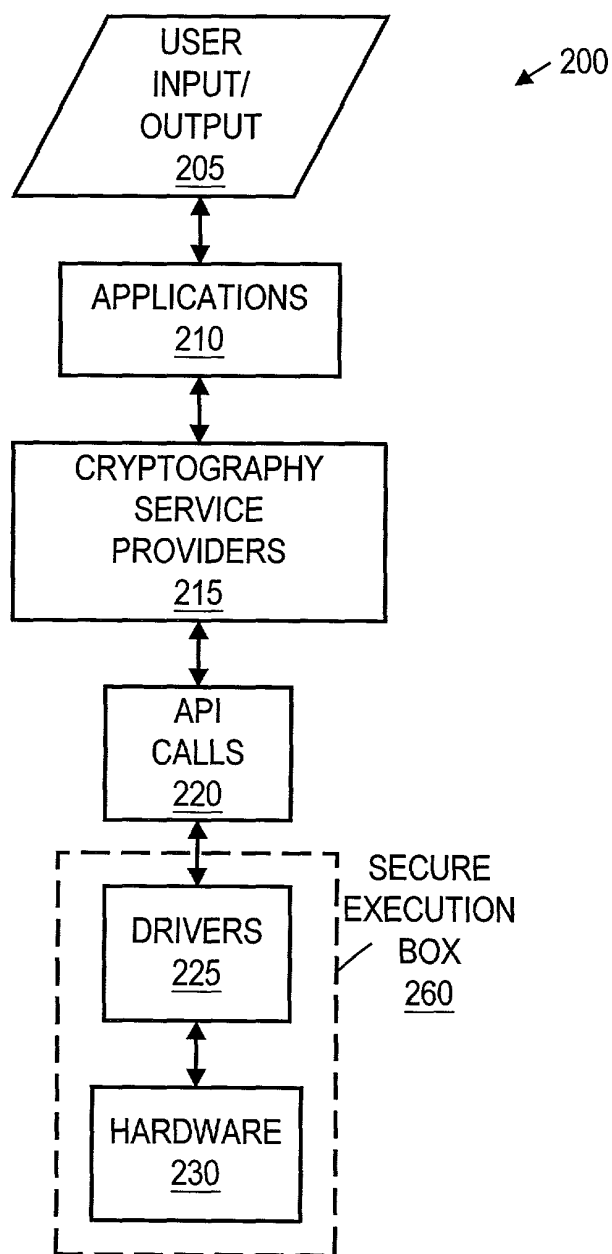


Fig. 3

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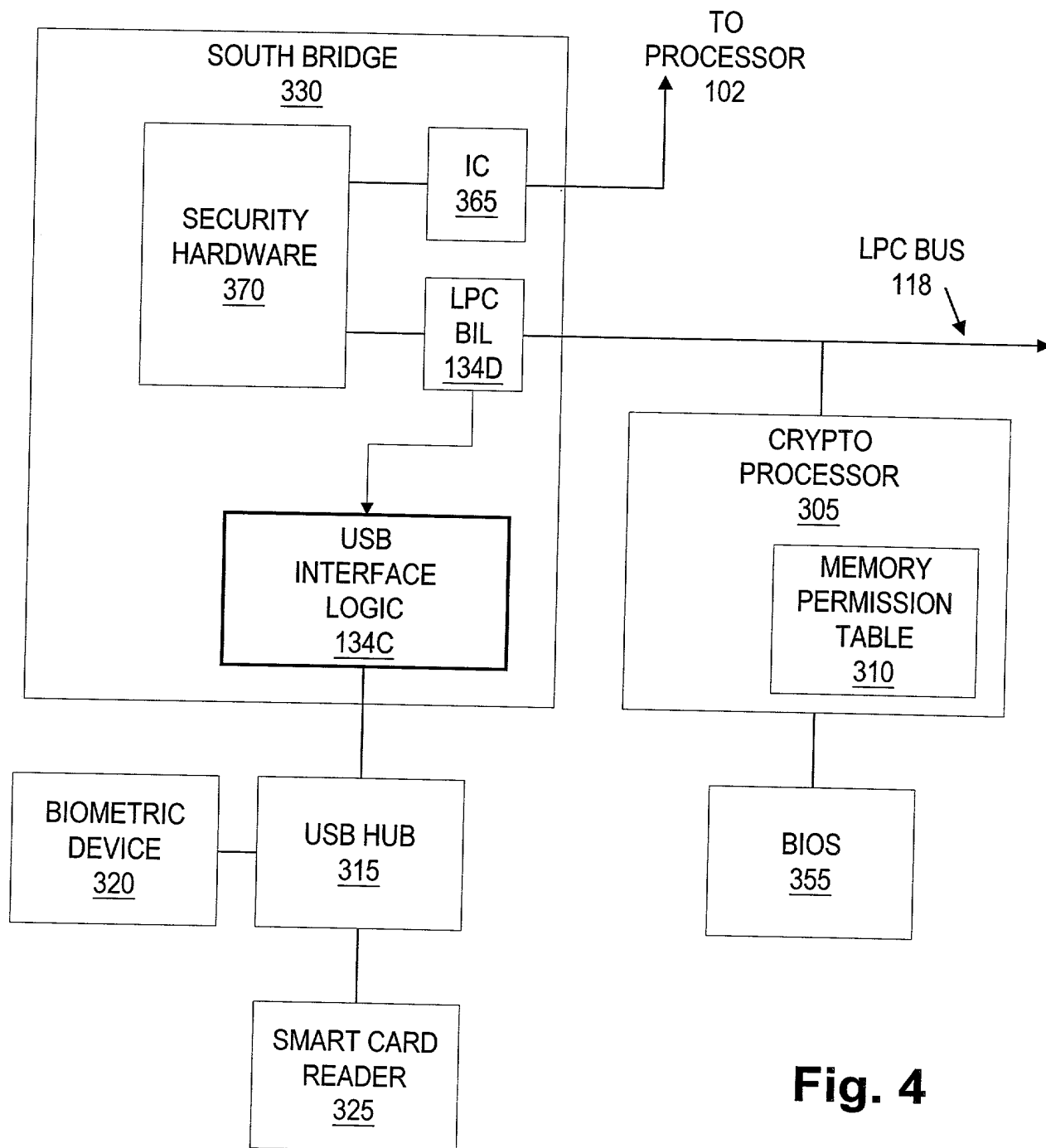


Fig. 4

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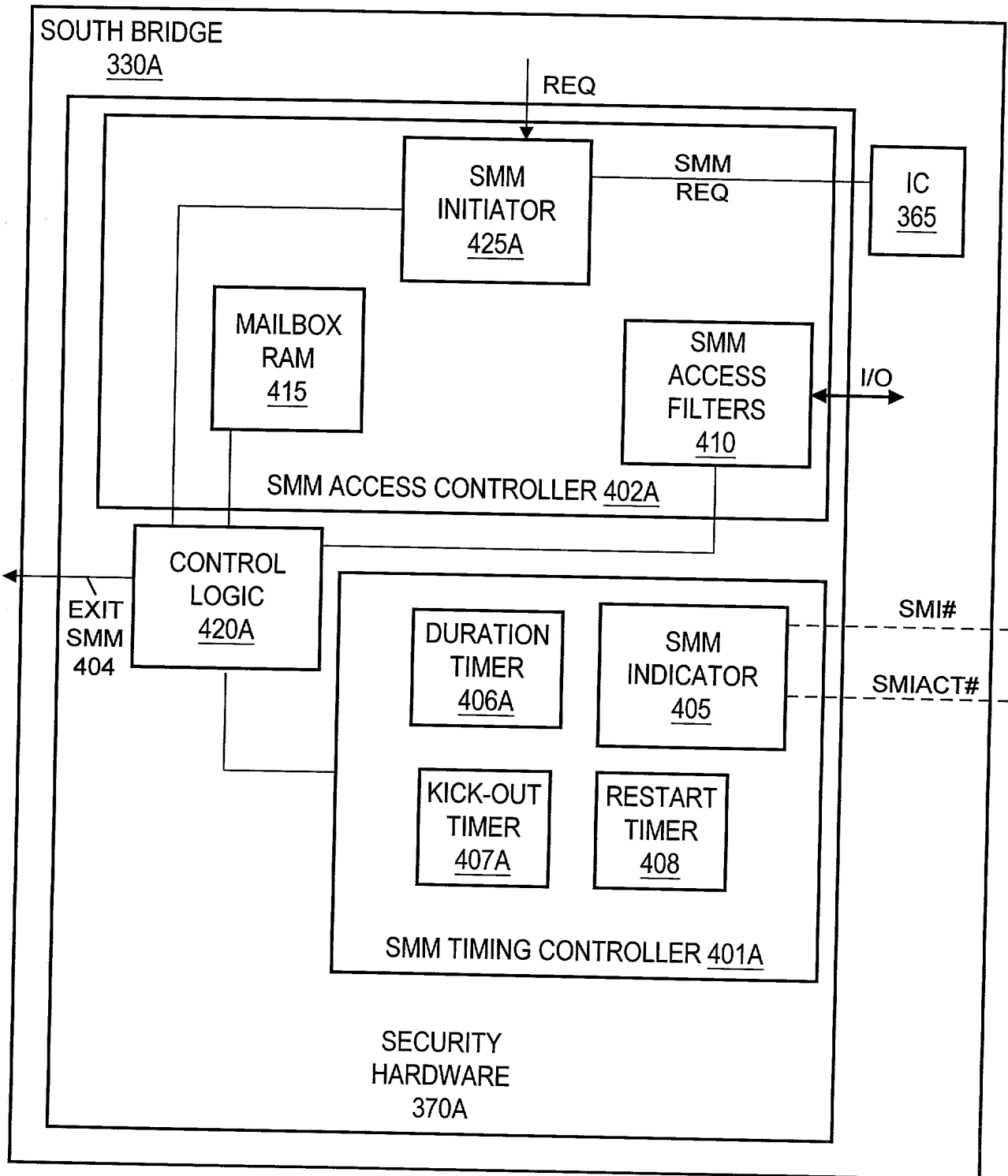


Fig. 5A

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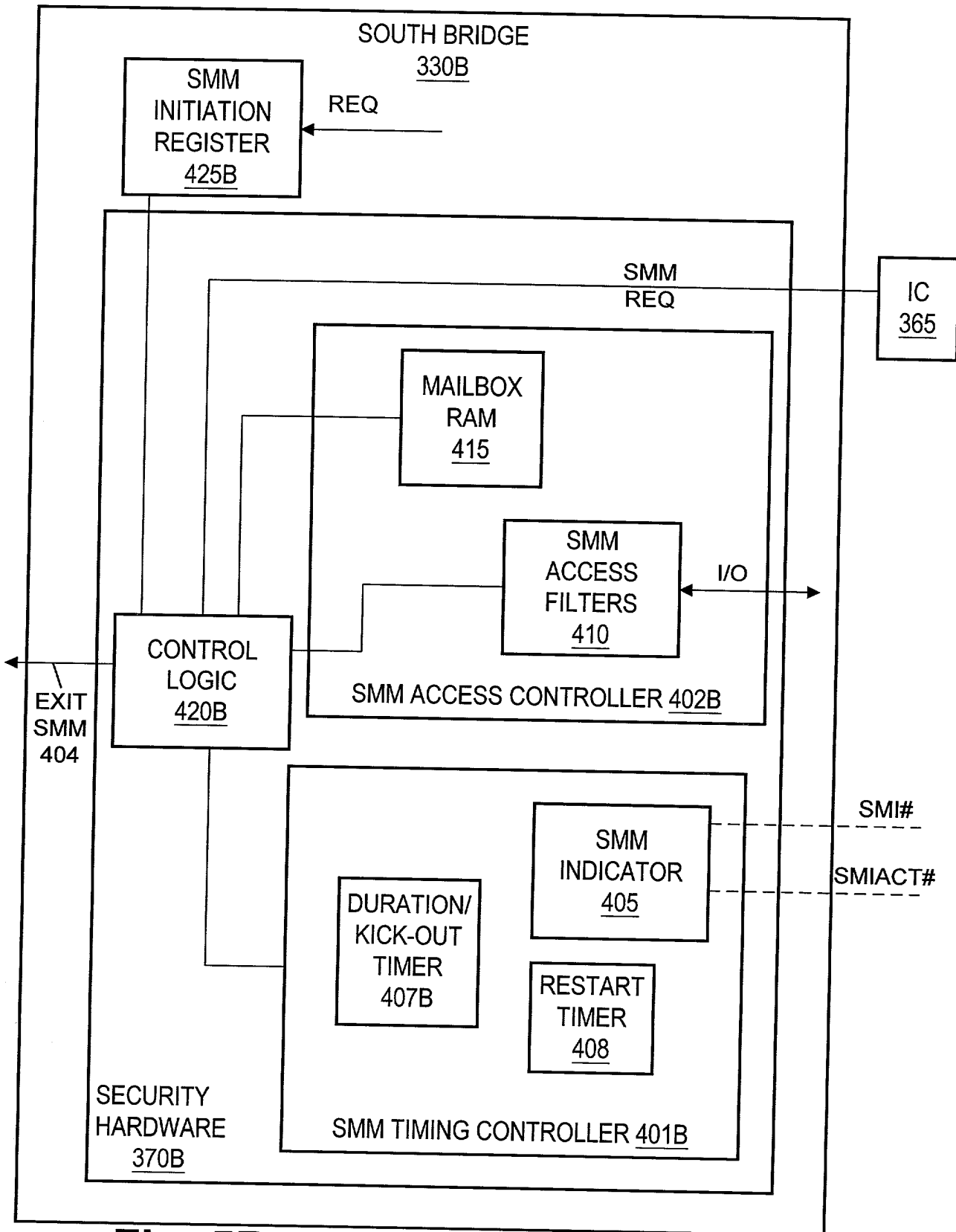


Fig. 5B

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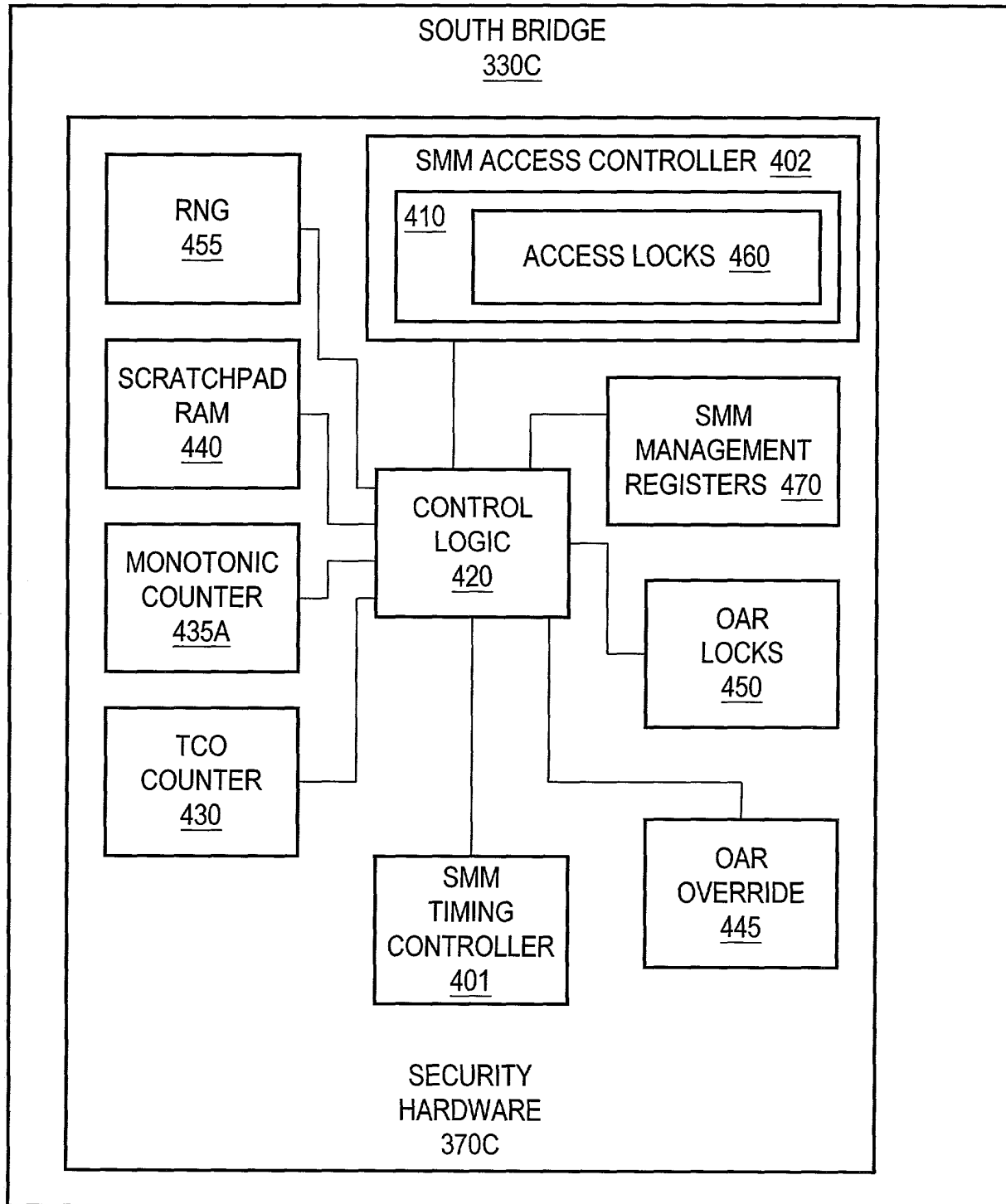


Fig. 6

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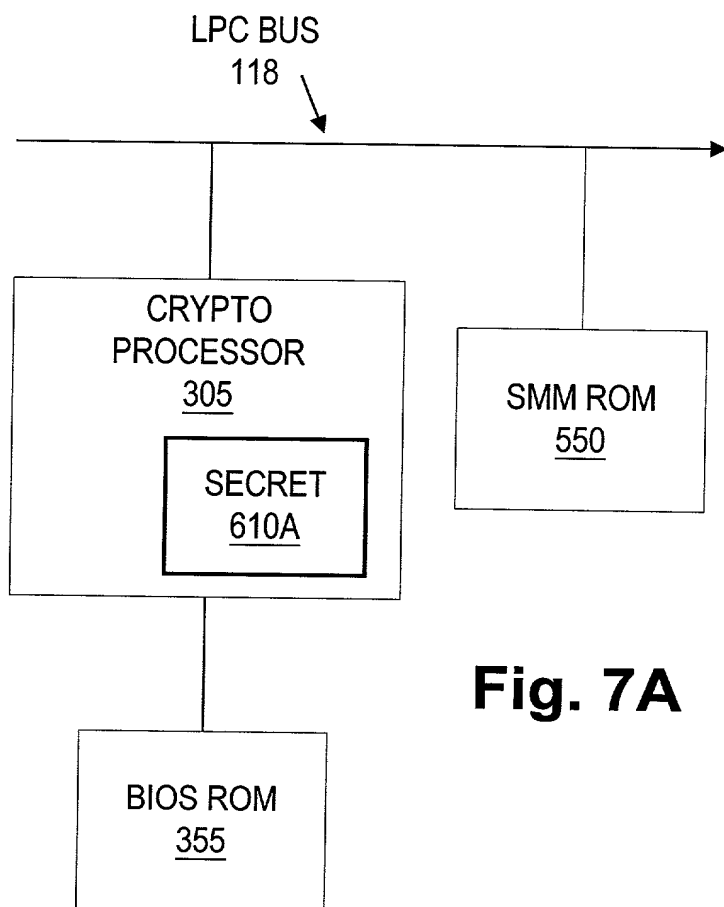


Fig. 7A

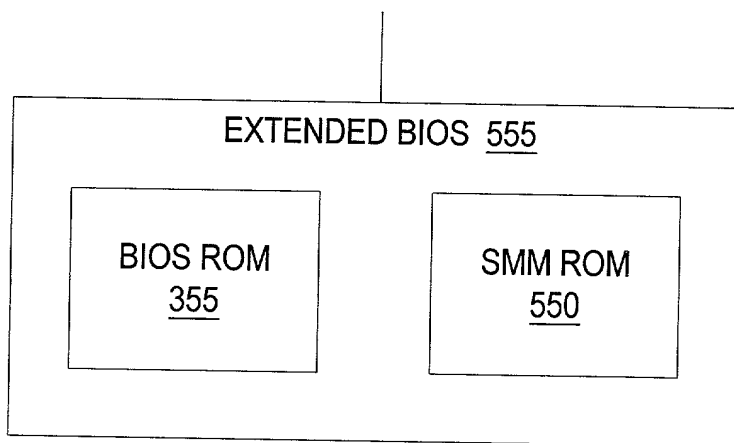


Fig. 7B

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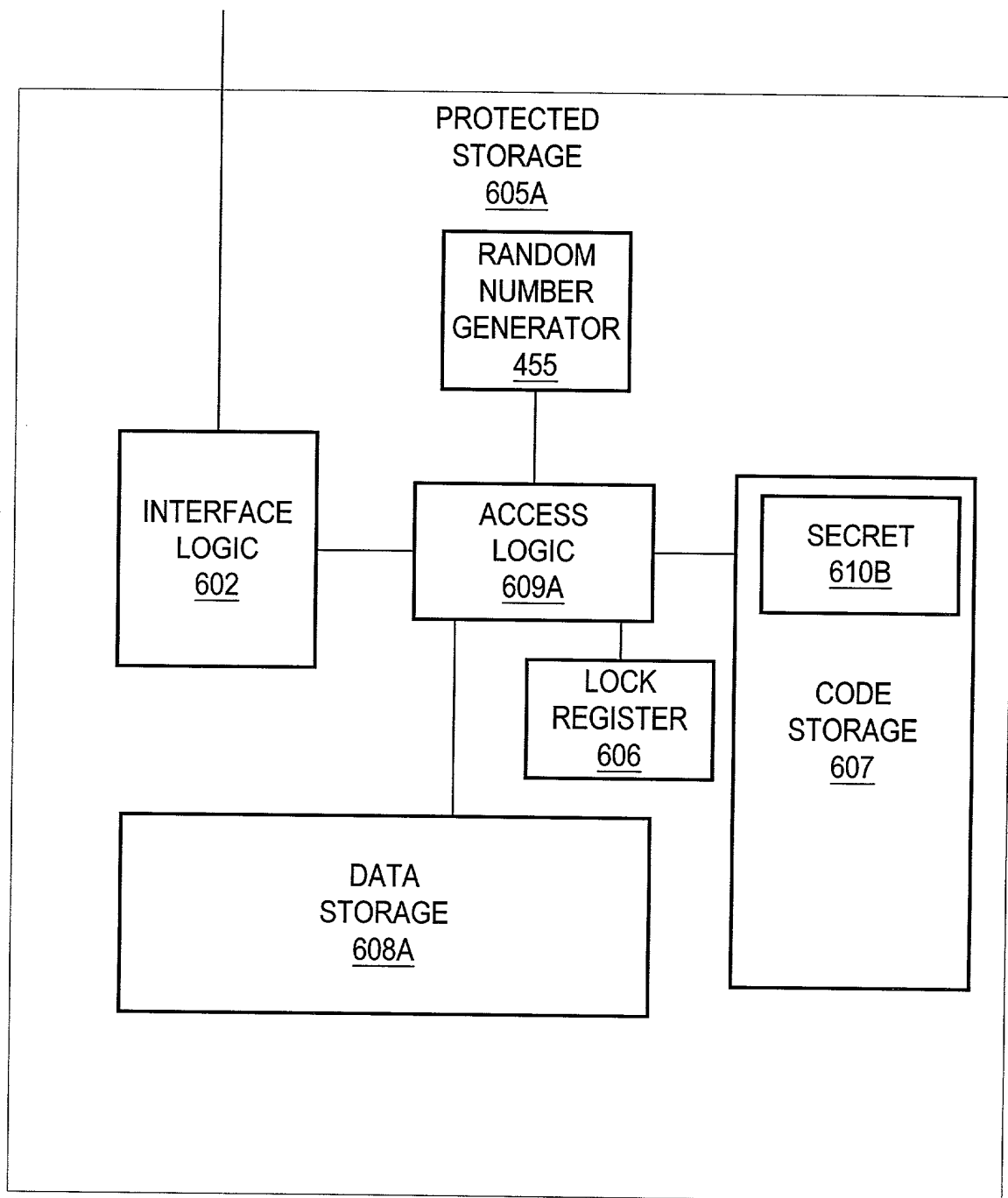


Fig. 7C

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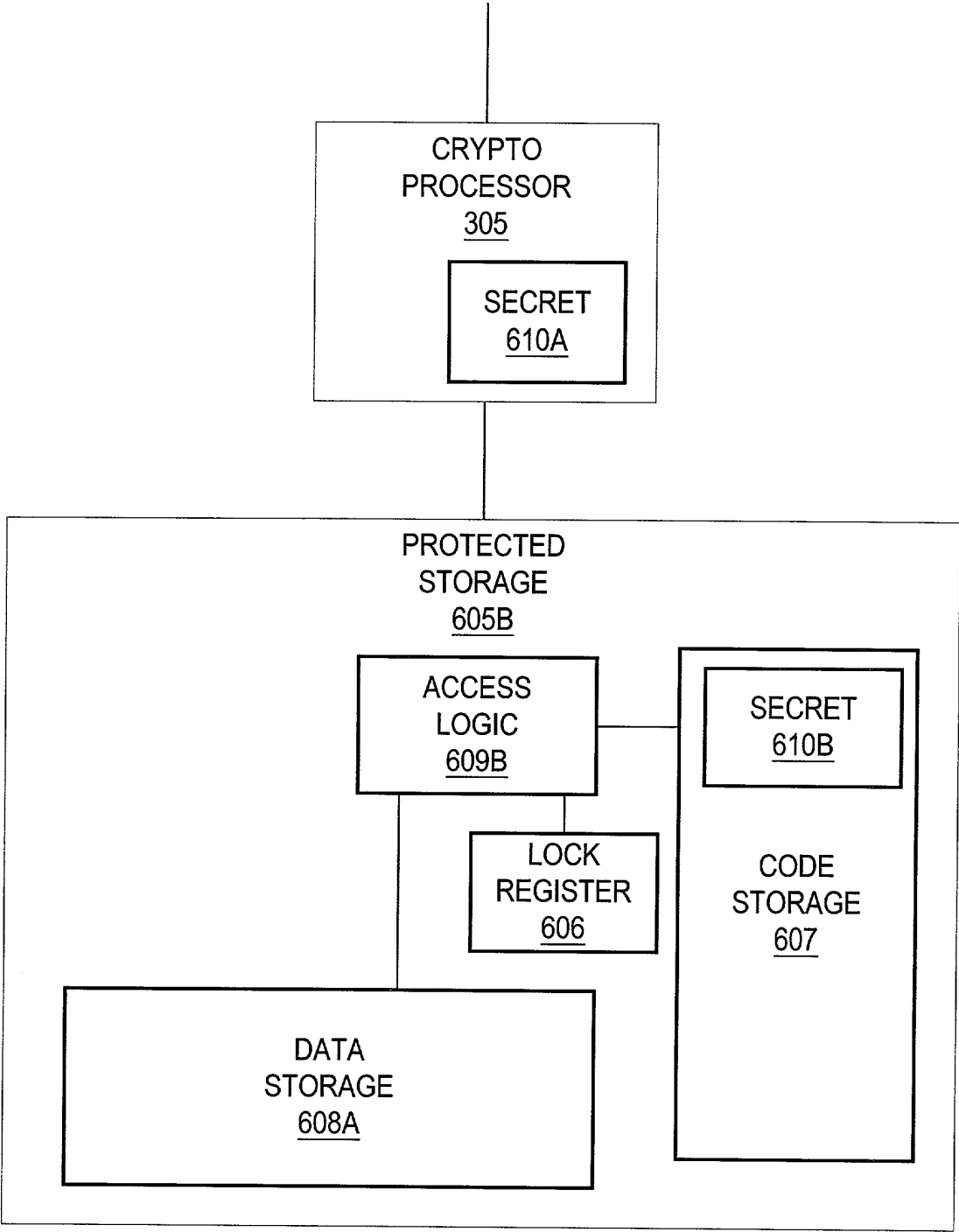


Fig. 7D

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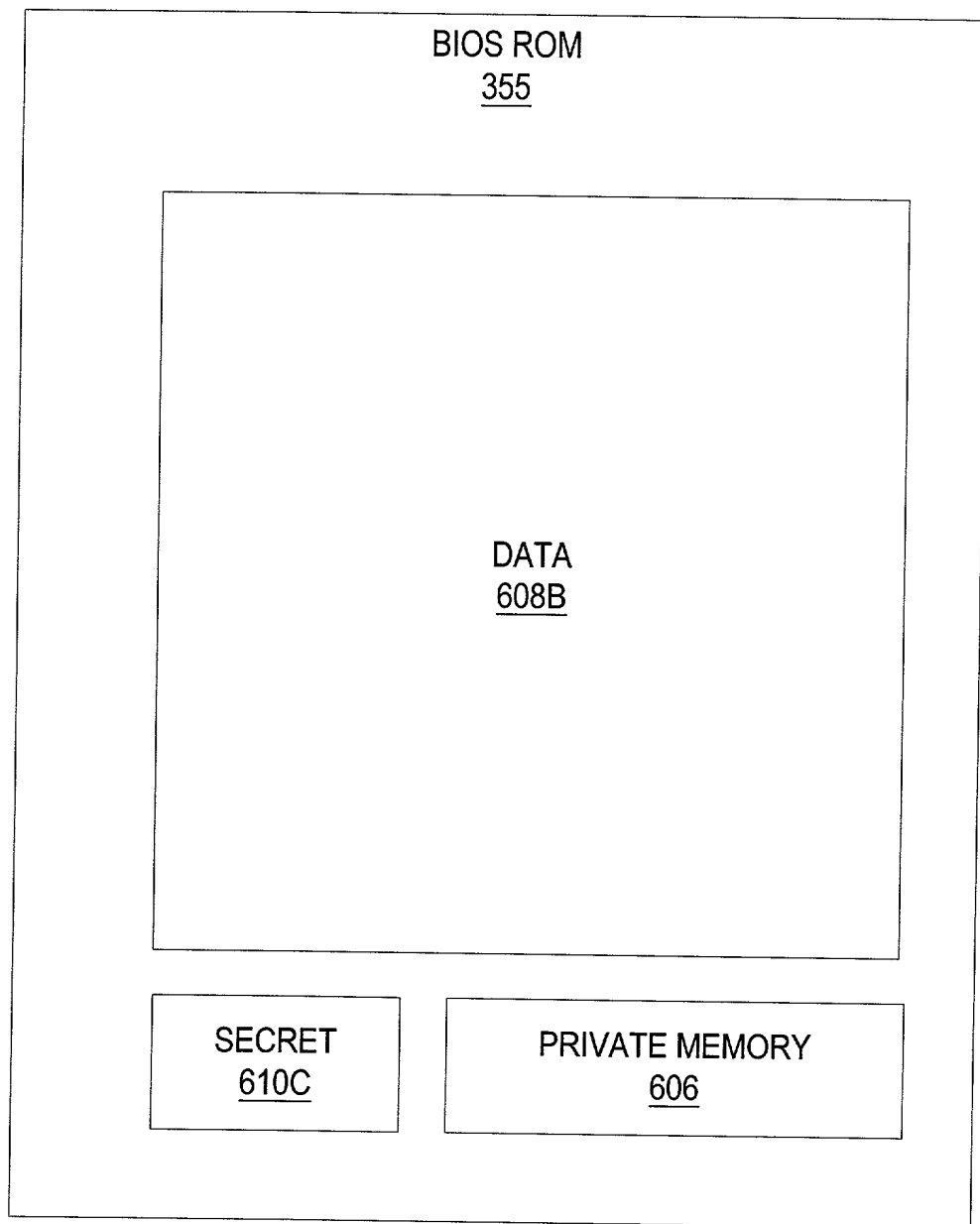


Fig. 8A

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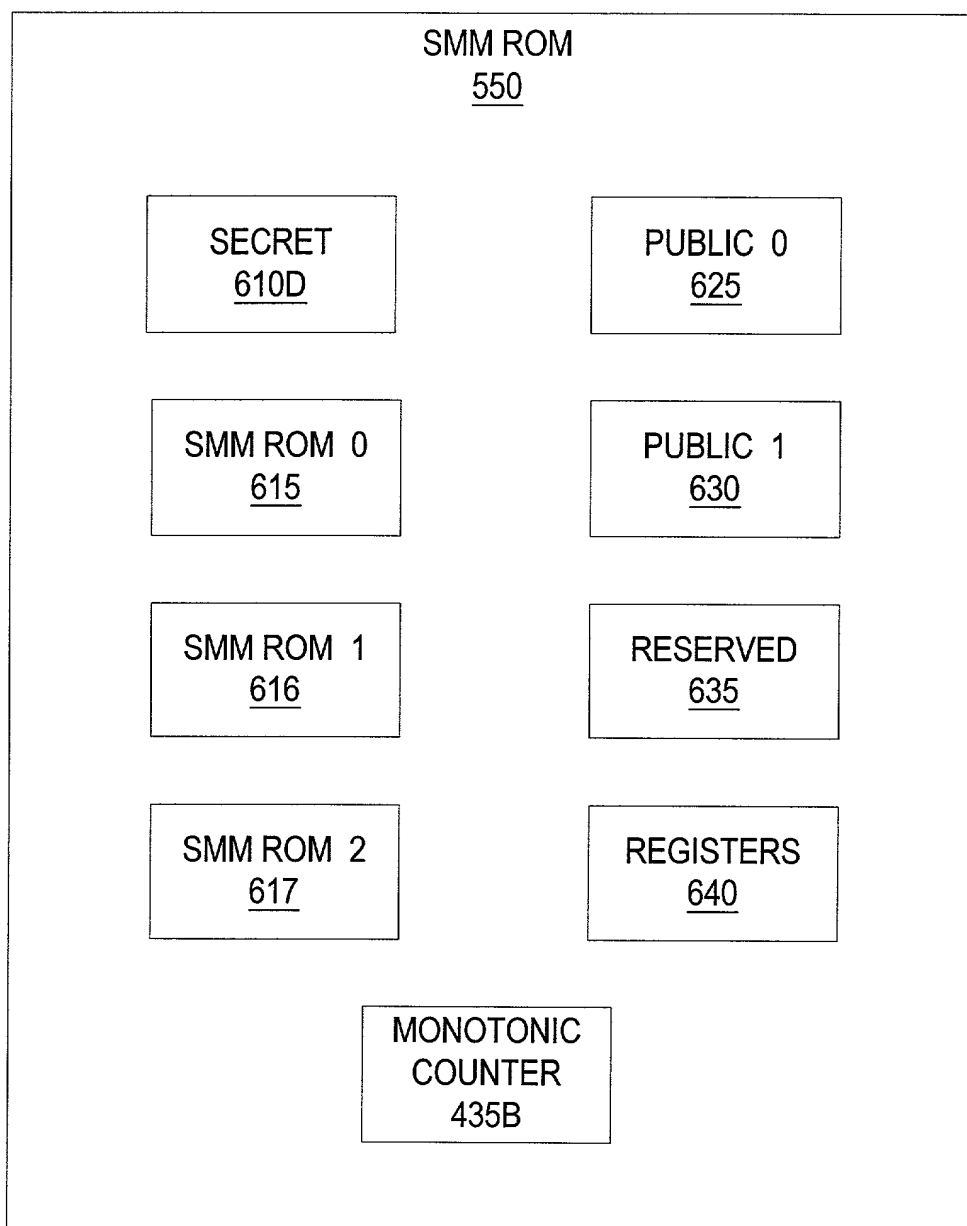


Fig. 8B

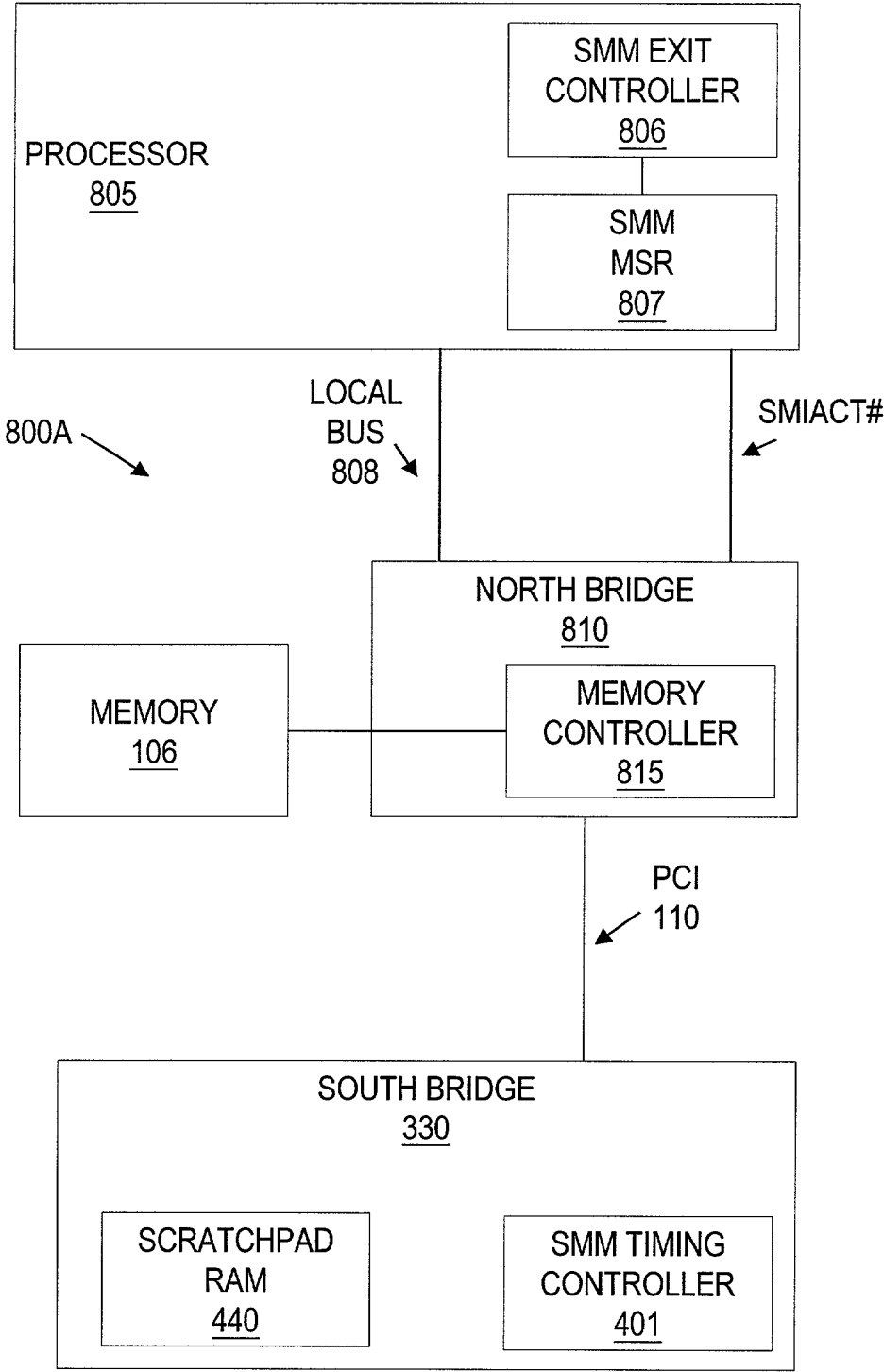


Fig. 9A

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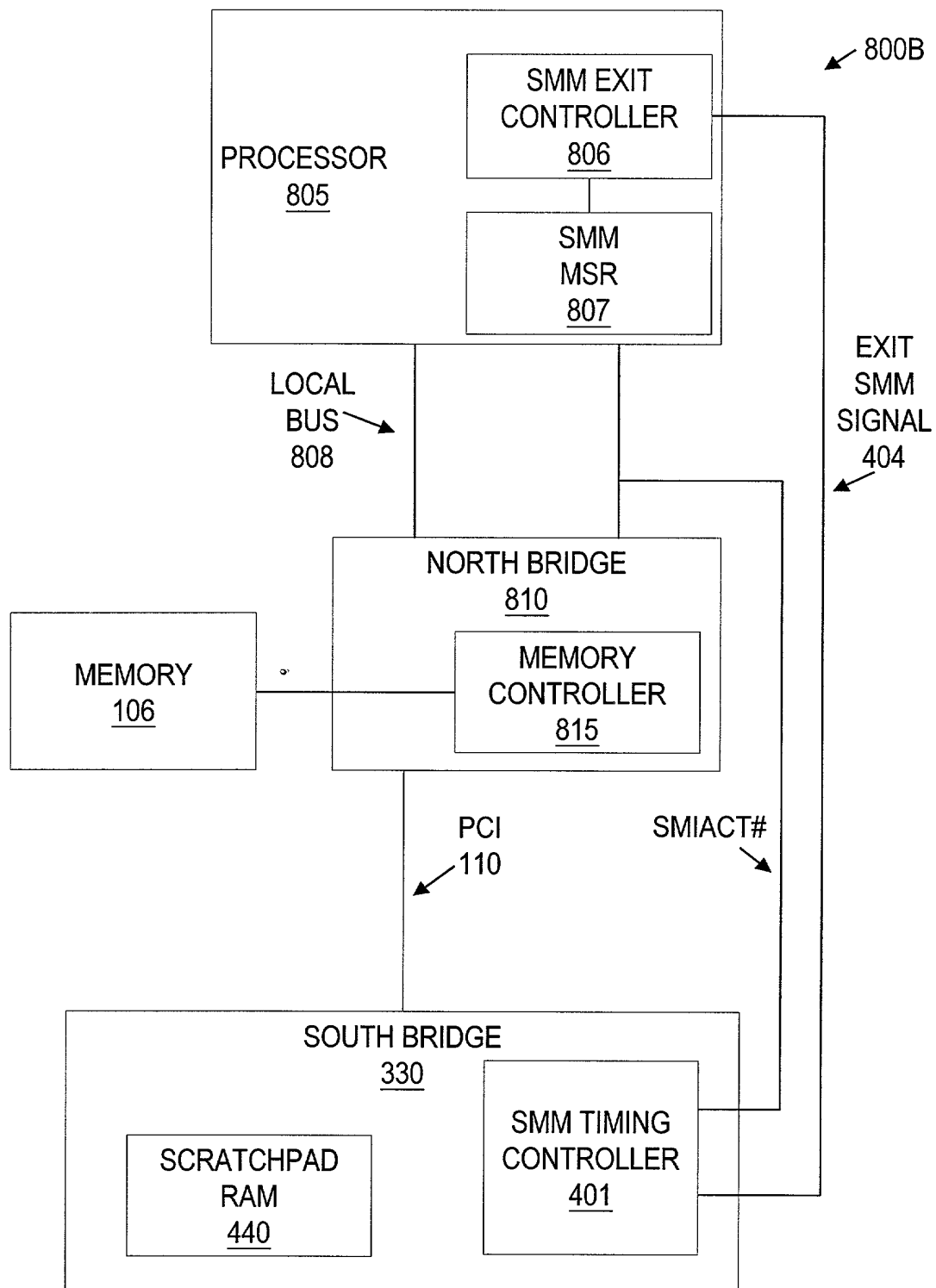


Fig. 9B

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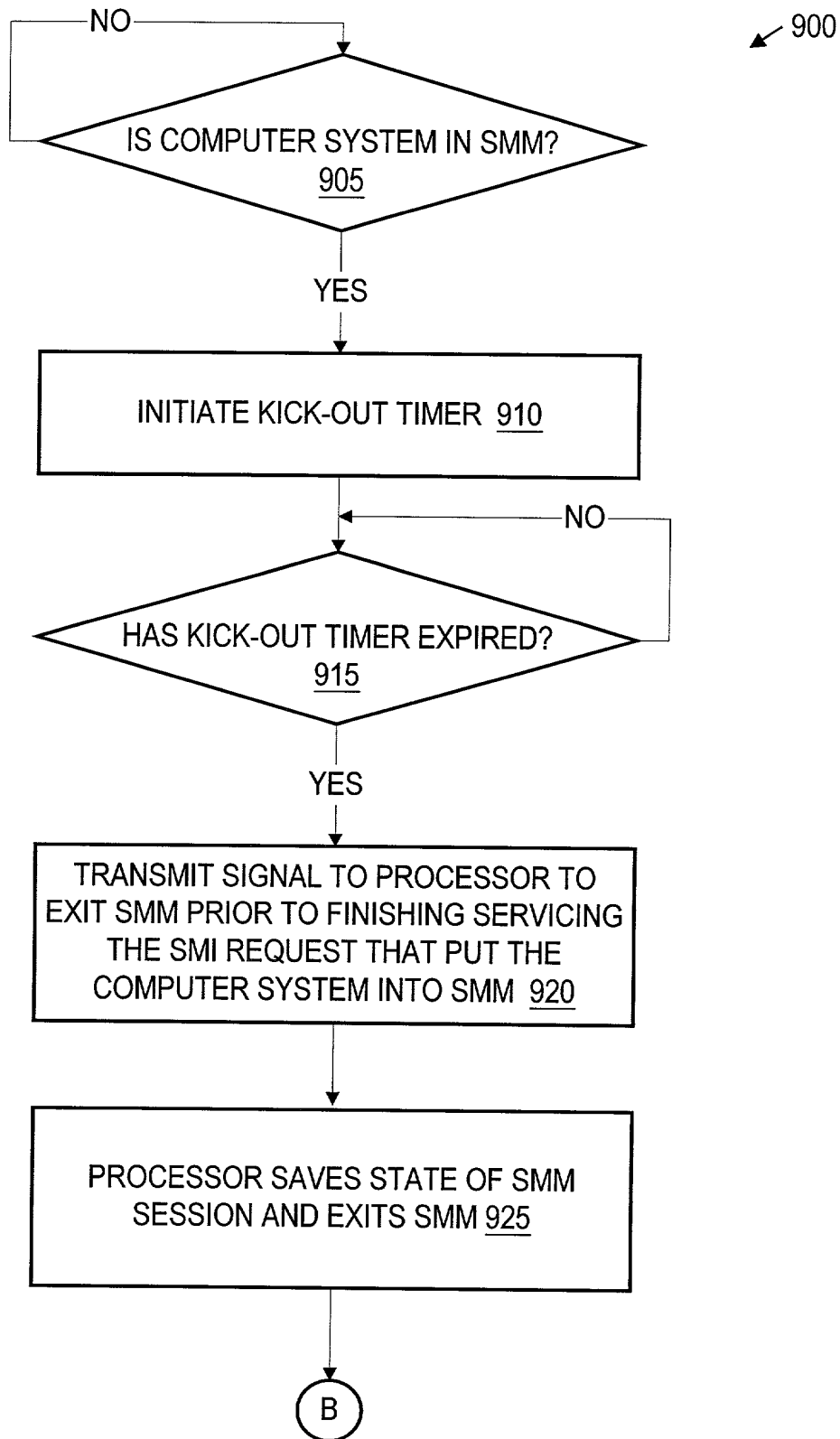


Fig. 10A

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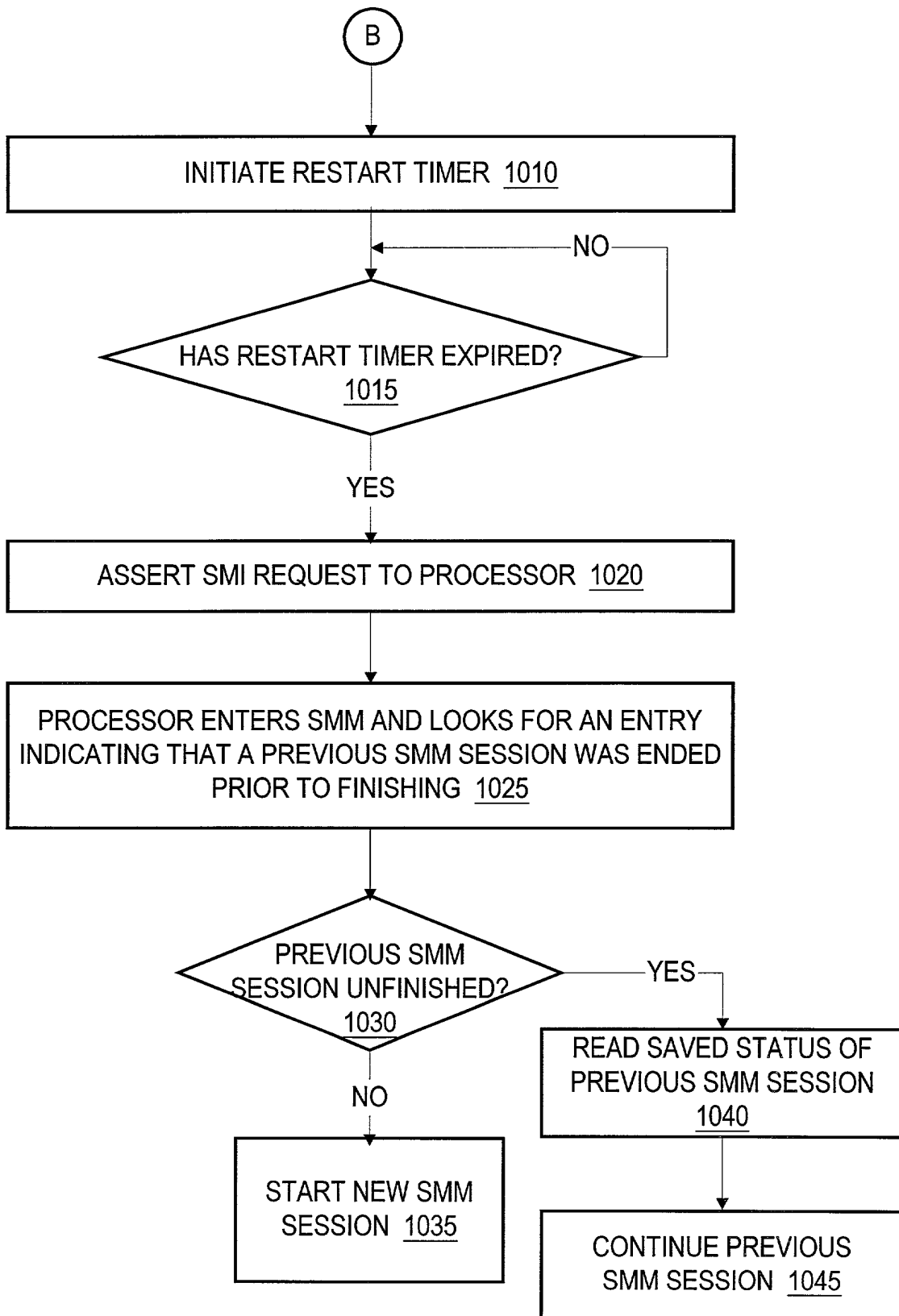


Fig. 10B

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1100A

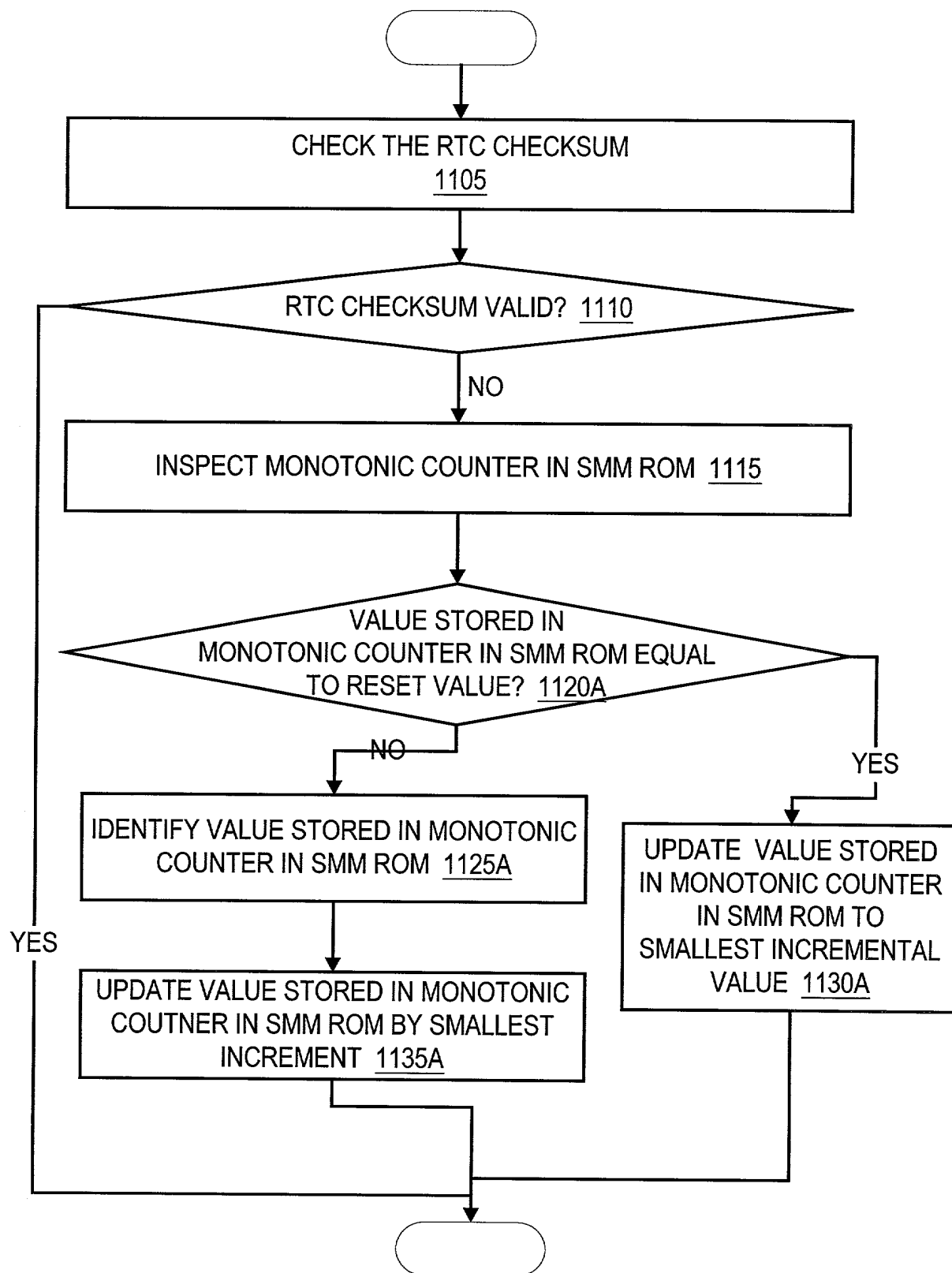


Fig. 11A

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1100B

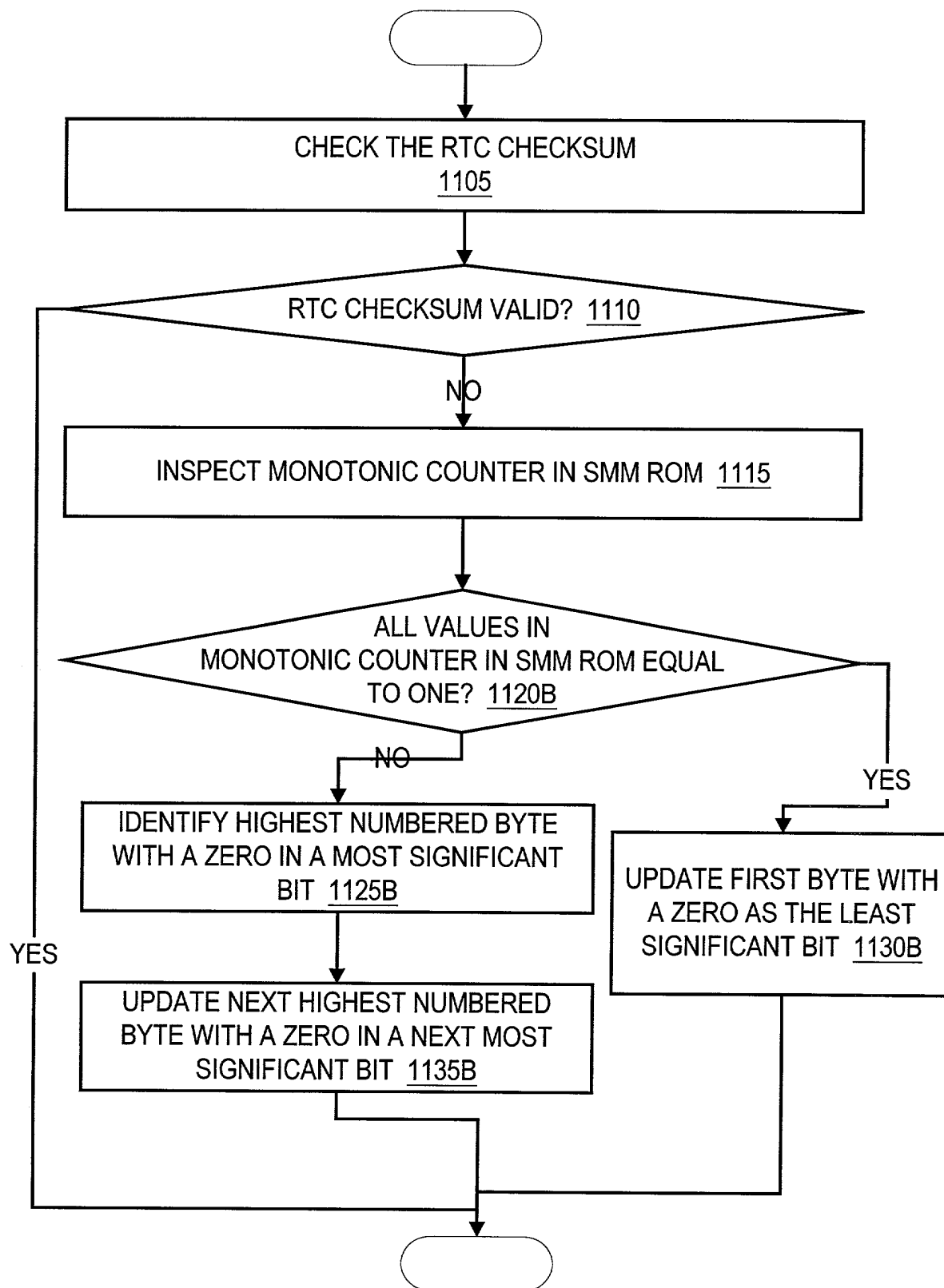


Fig. 11B

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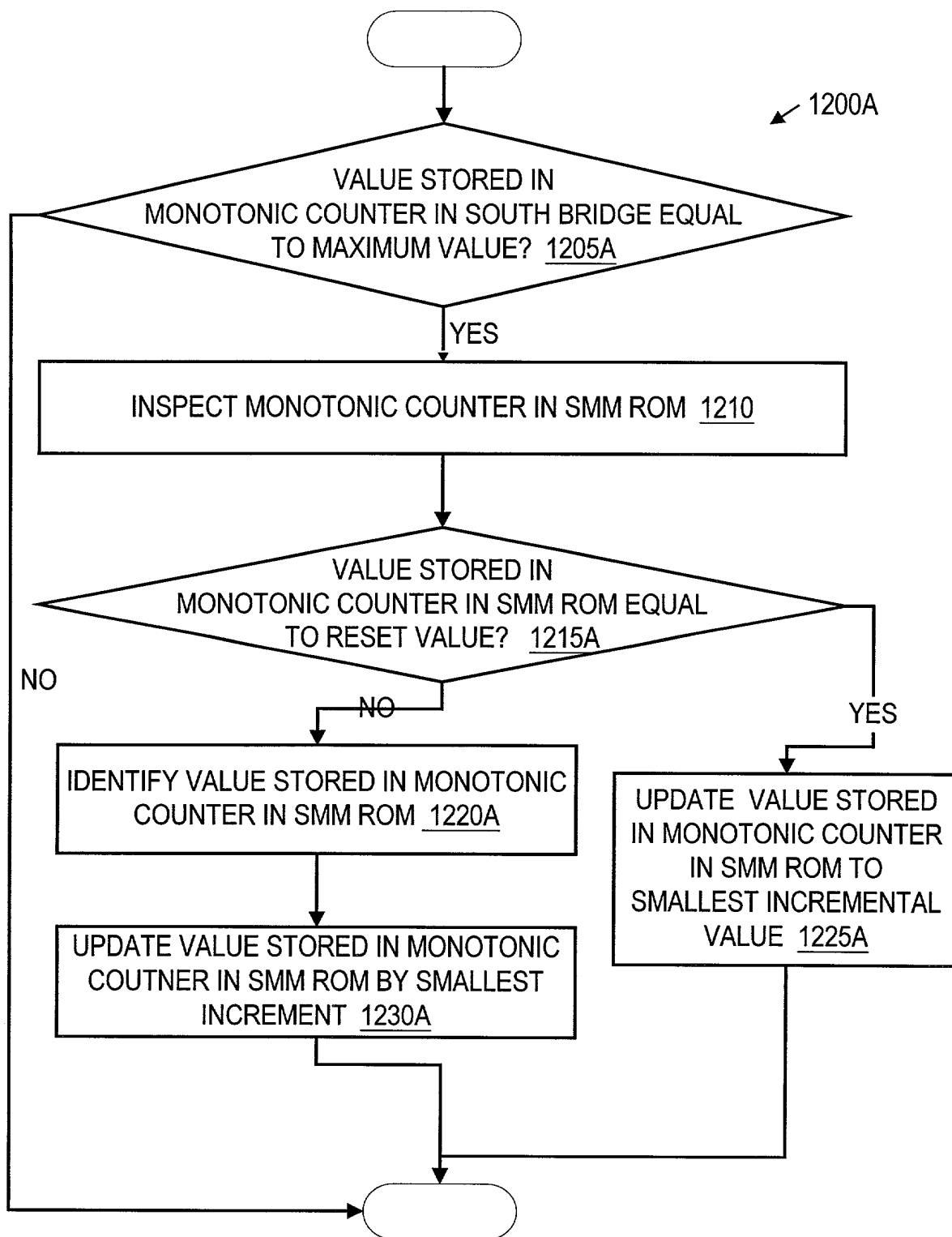


Fig. 12A

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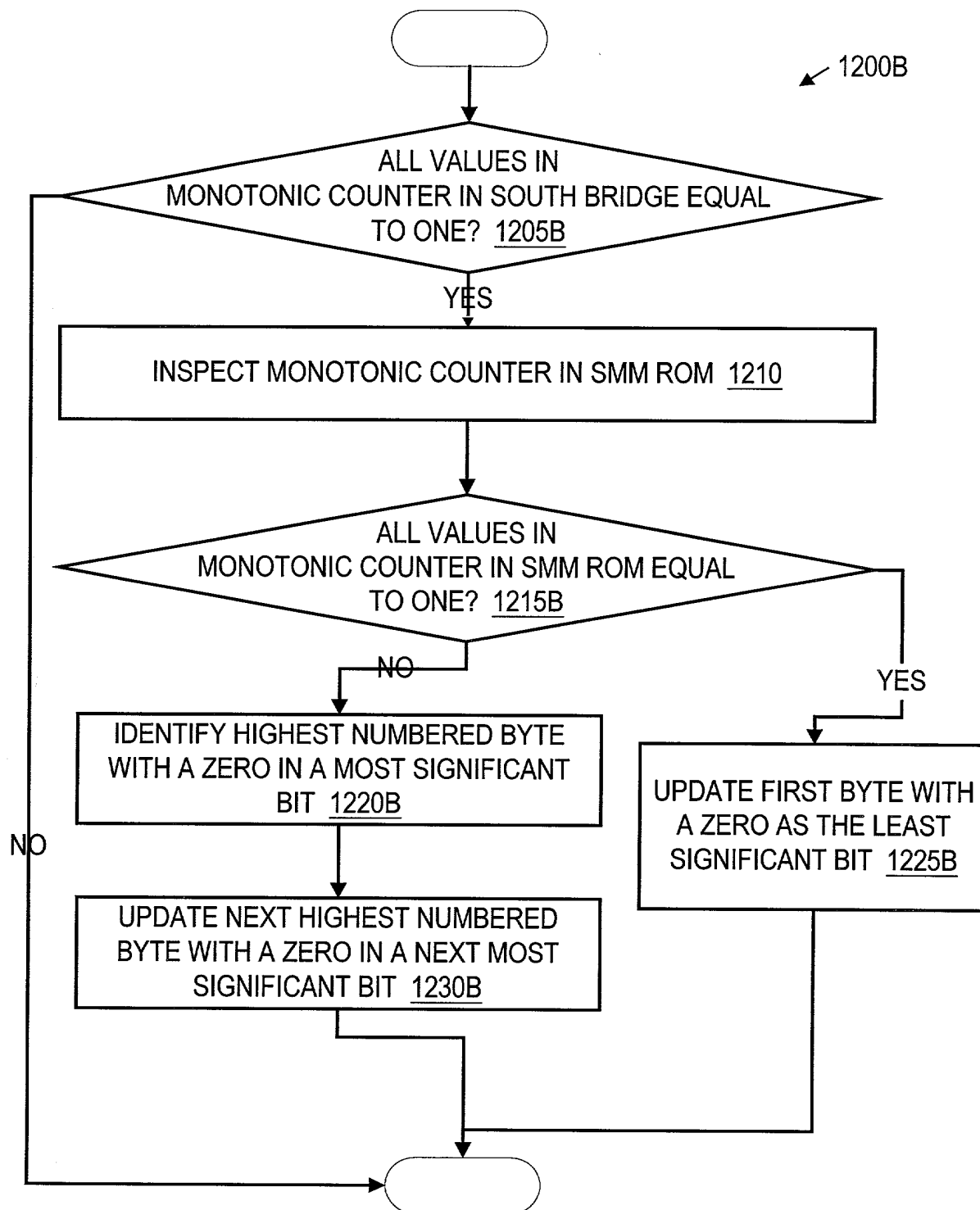


Fig. 12B

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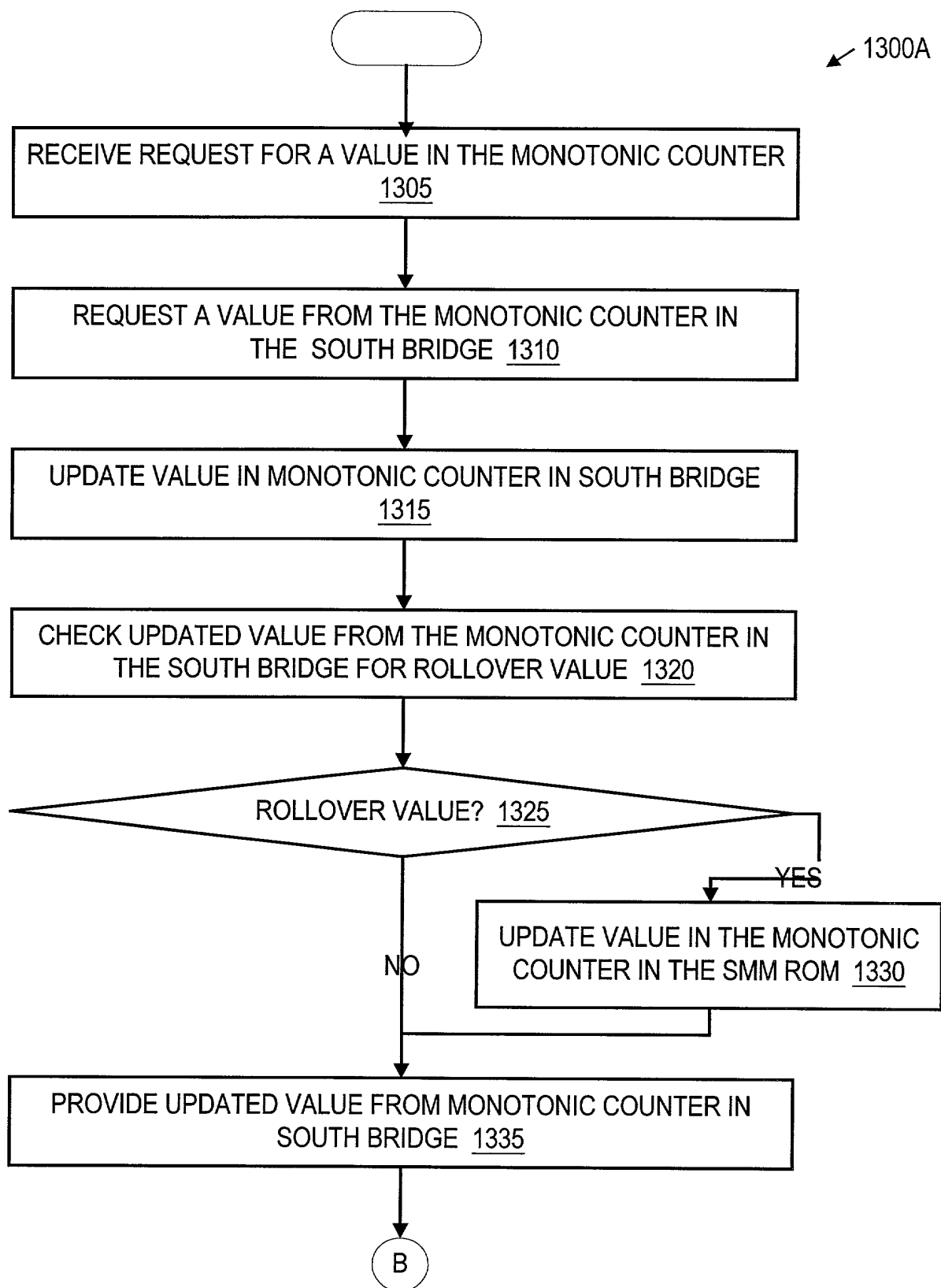


Fig. 13A

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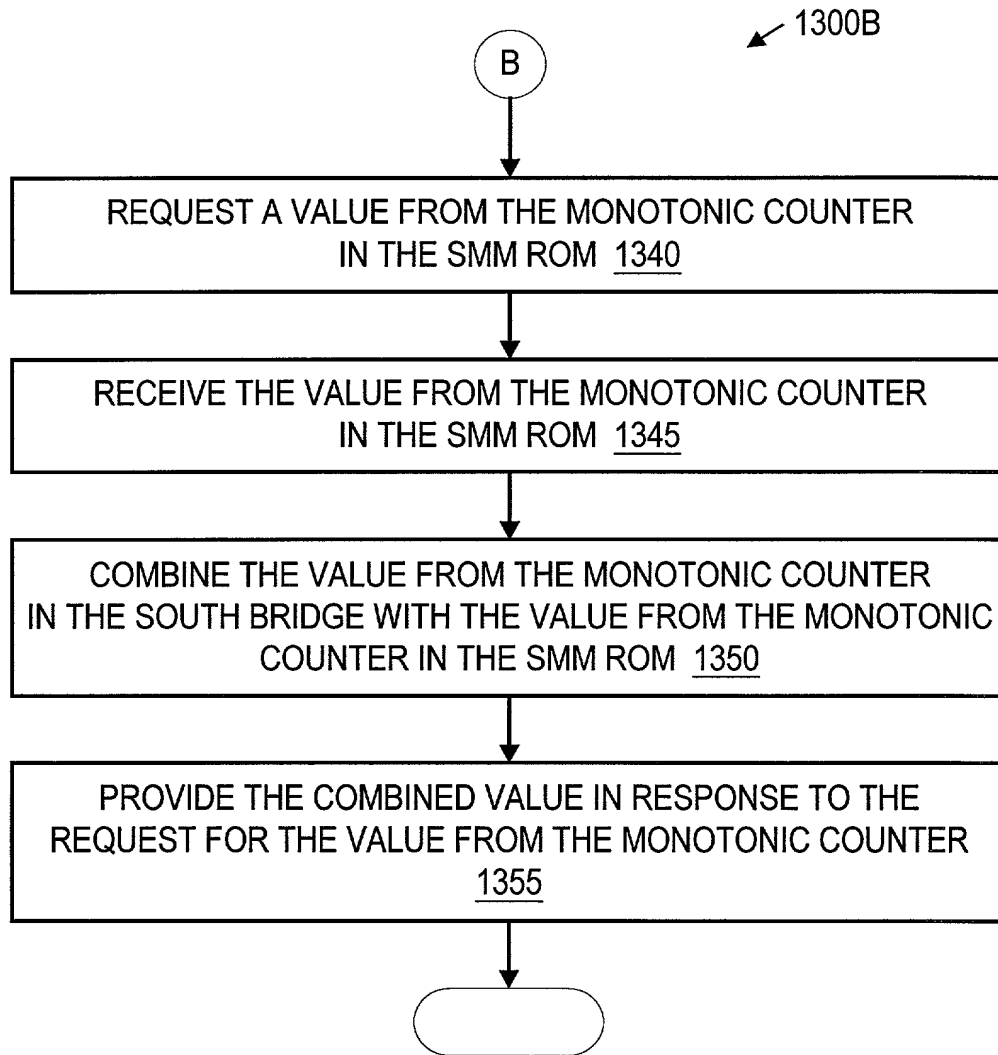


Fig. 13B

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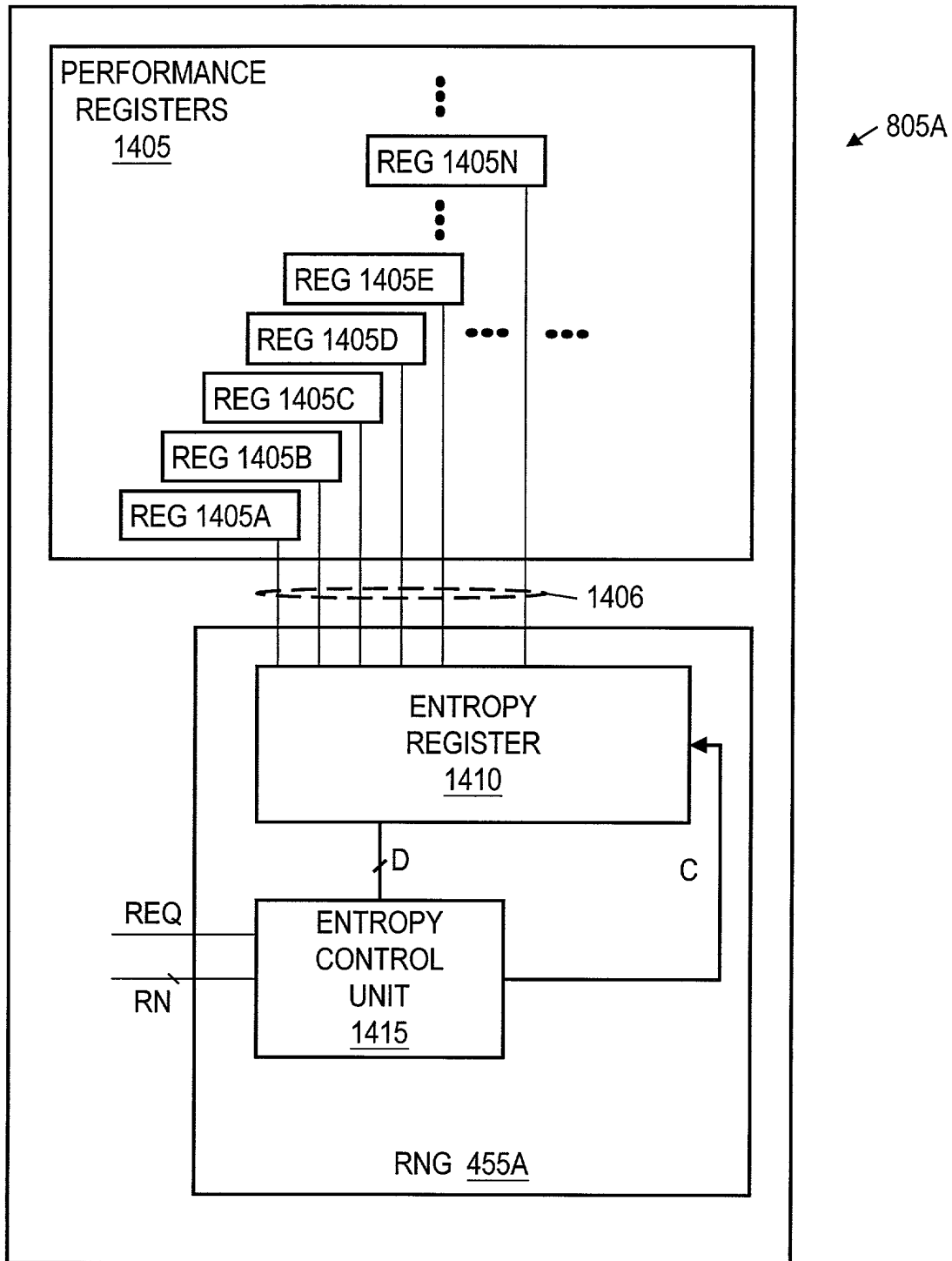


Fig. 14A

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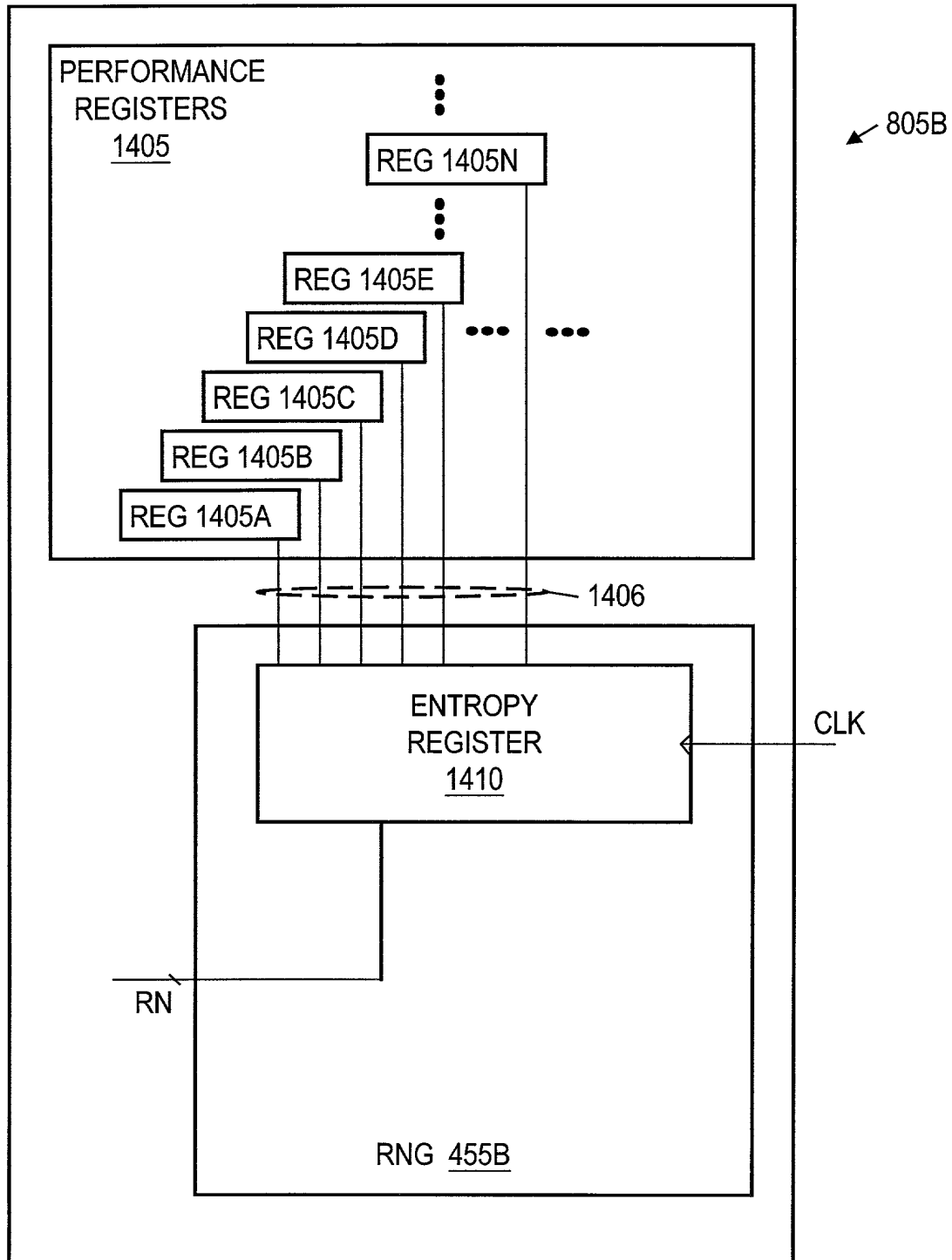


Fig. 14B

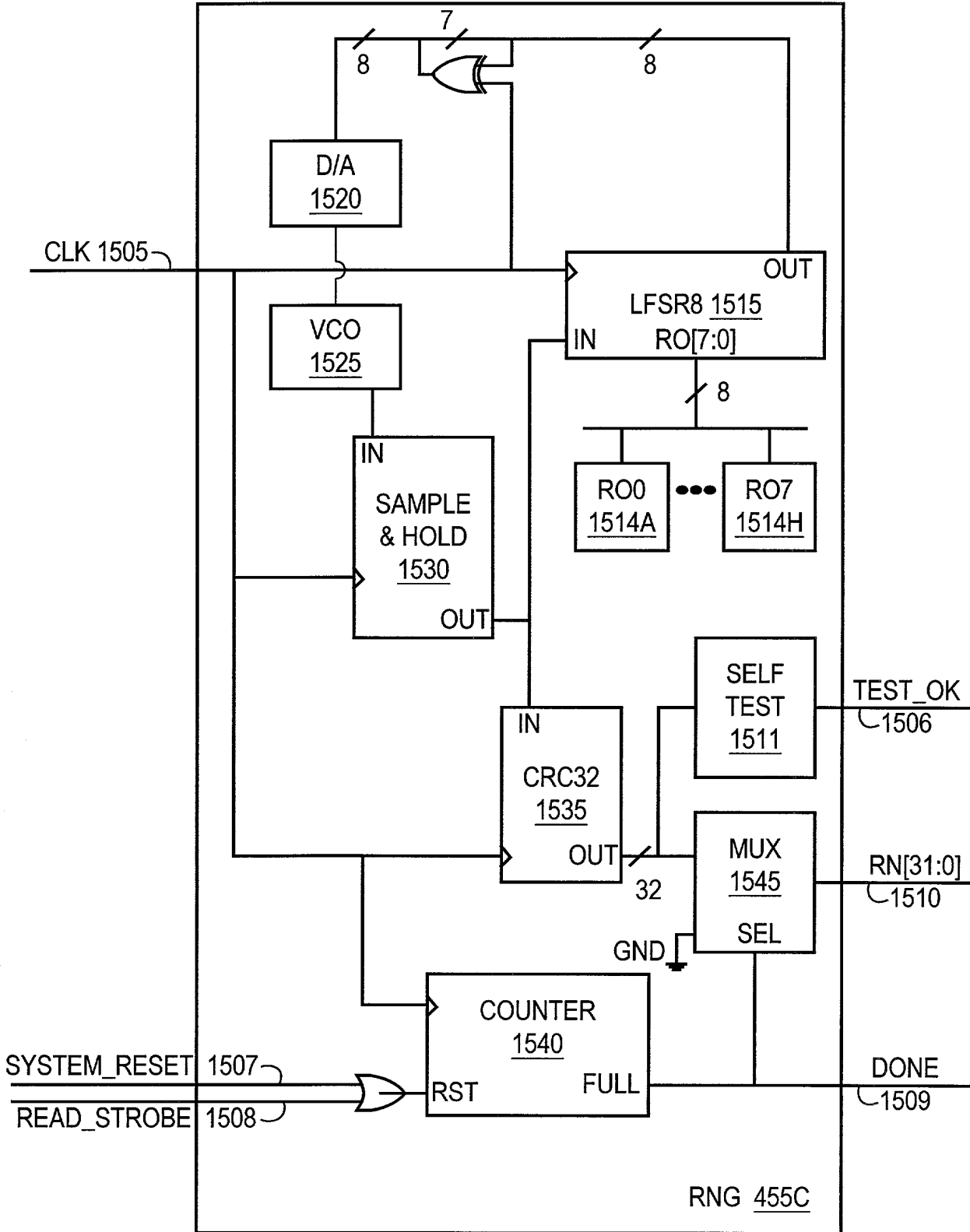


Fig. 15

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1600A

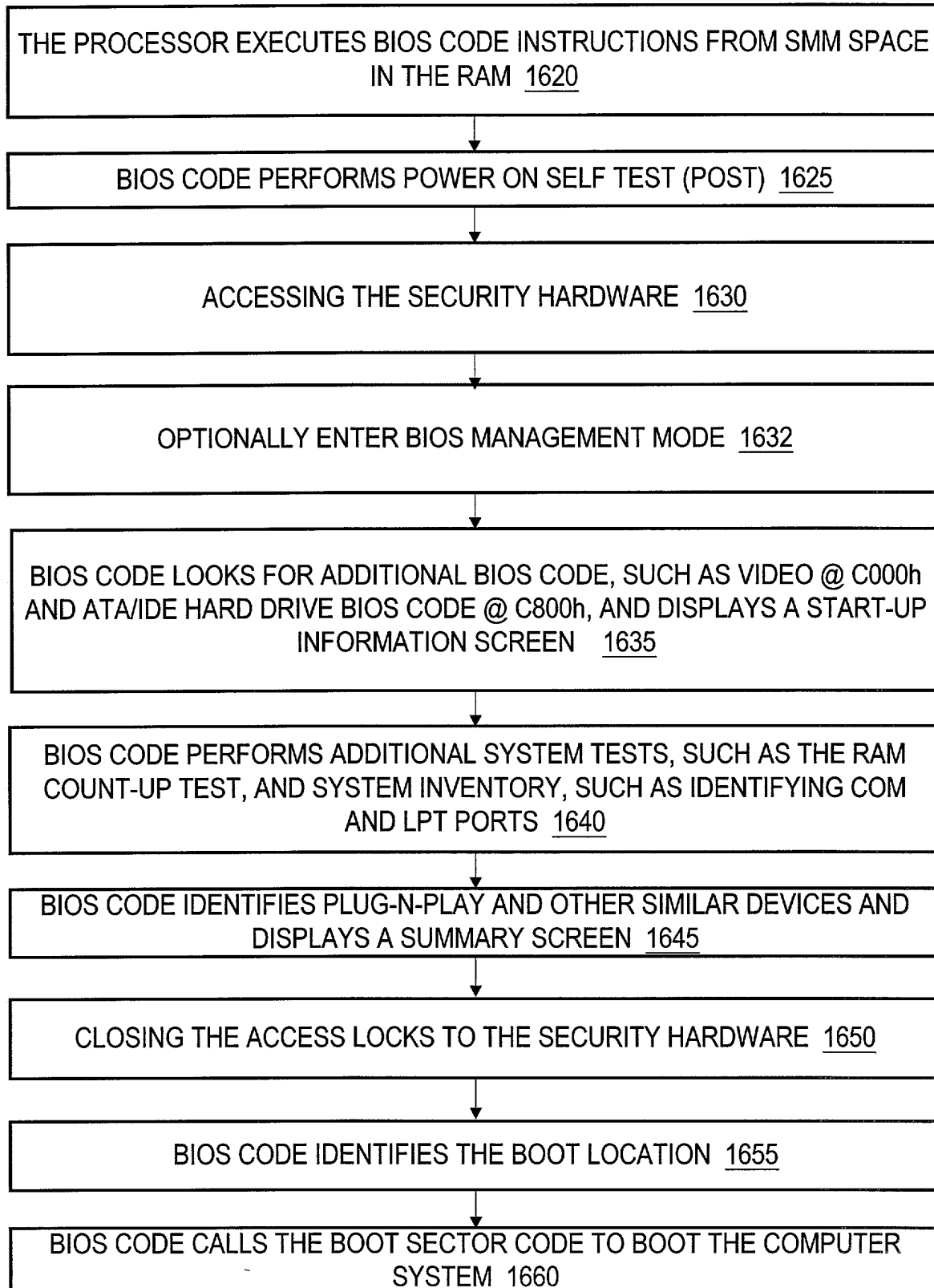


Fig. 16A

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1600B

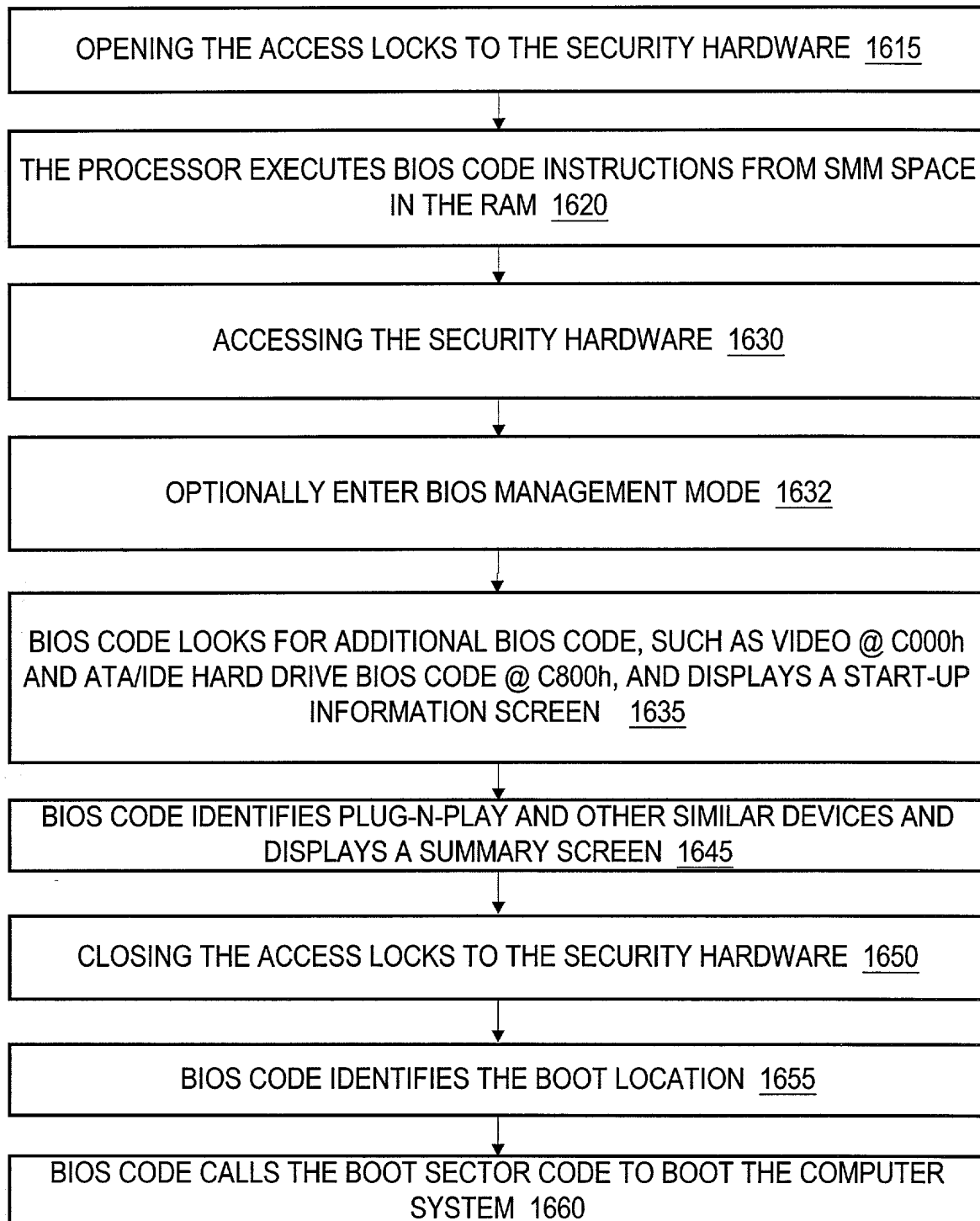


Fig. 16B

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1600C

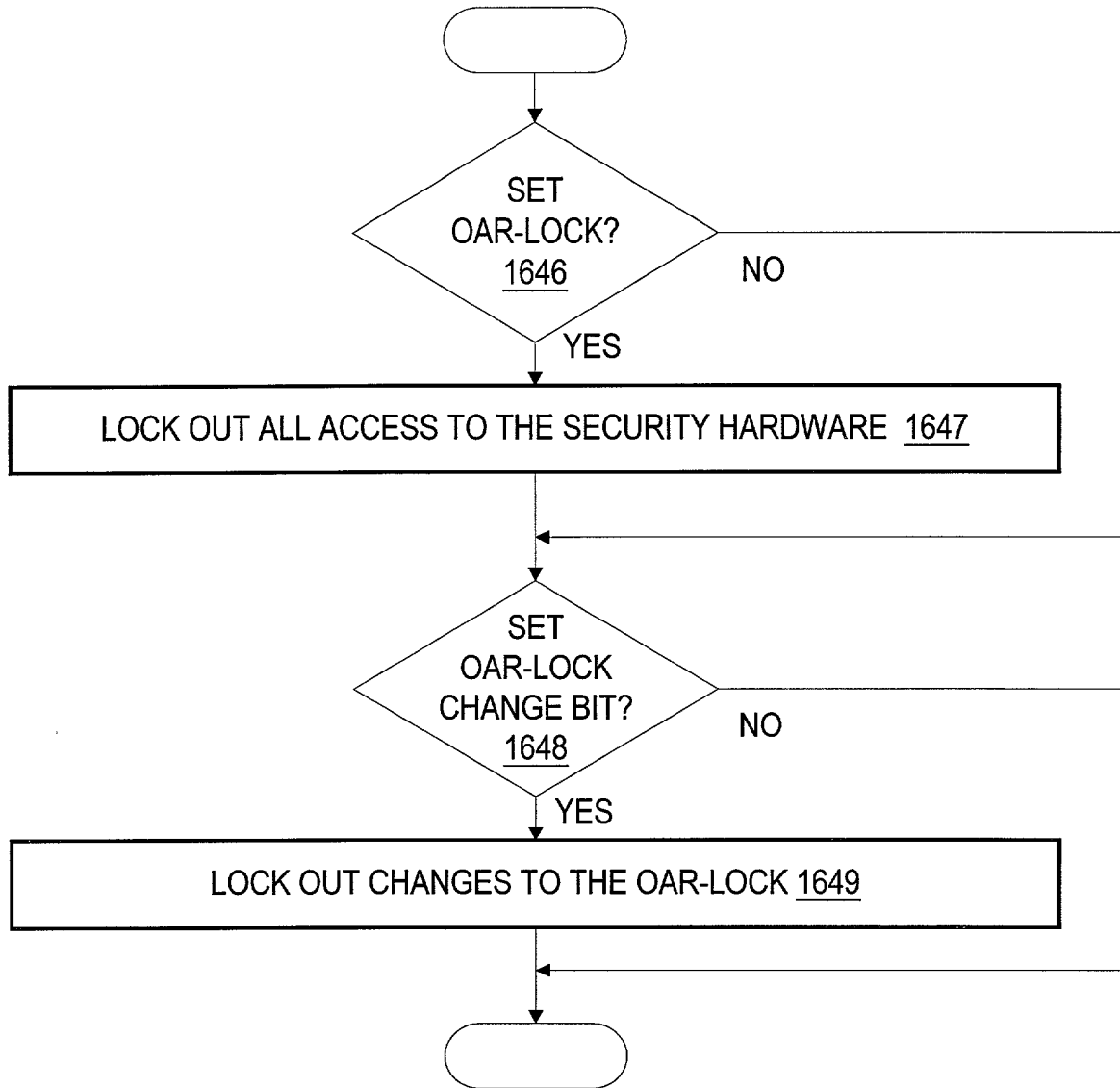


Fig. 16C

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1600D

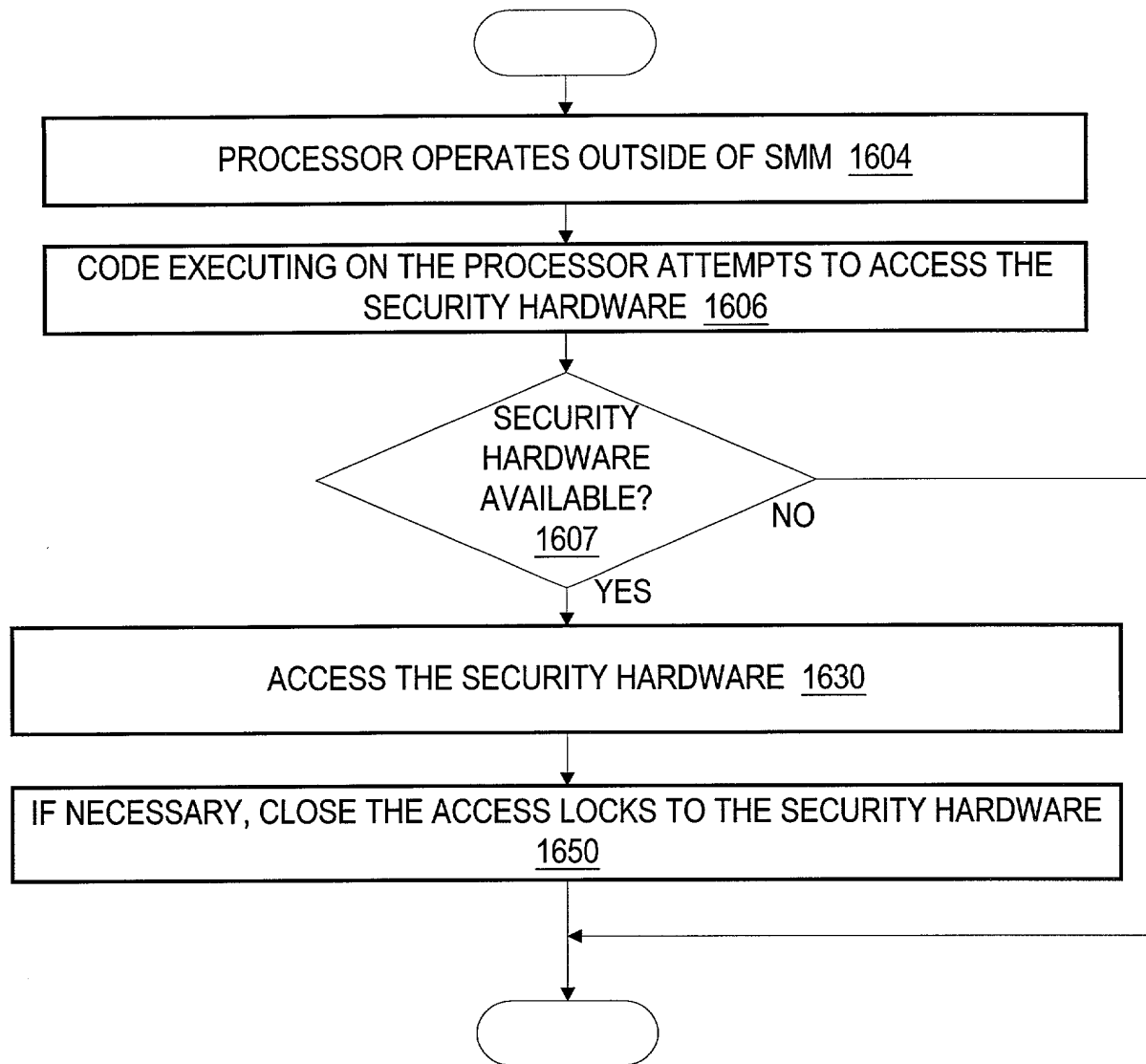


Fig. 16D

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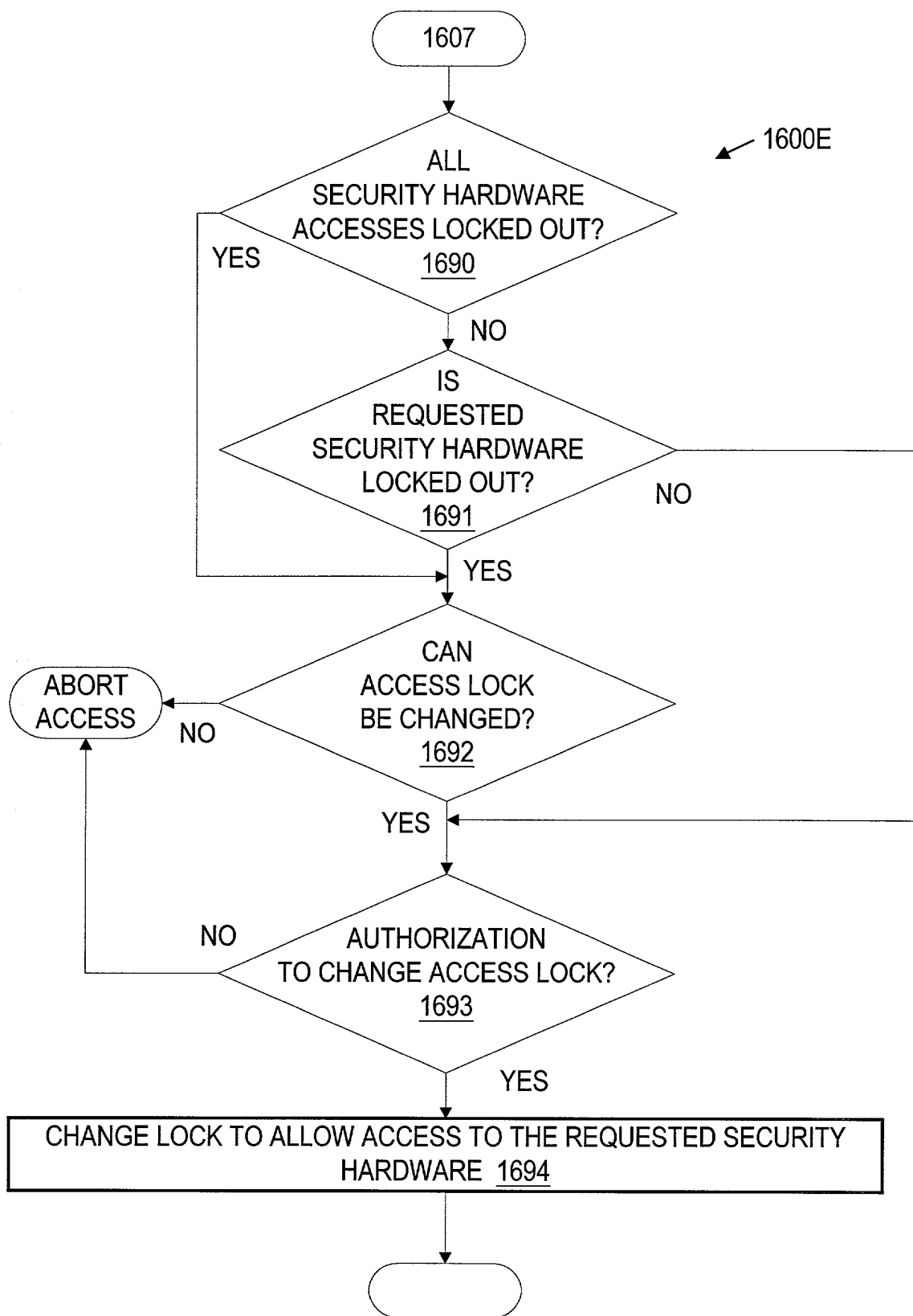


Fig. 16E

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1600F

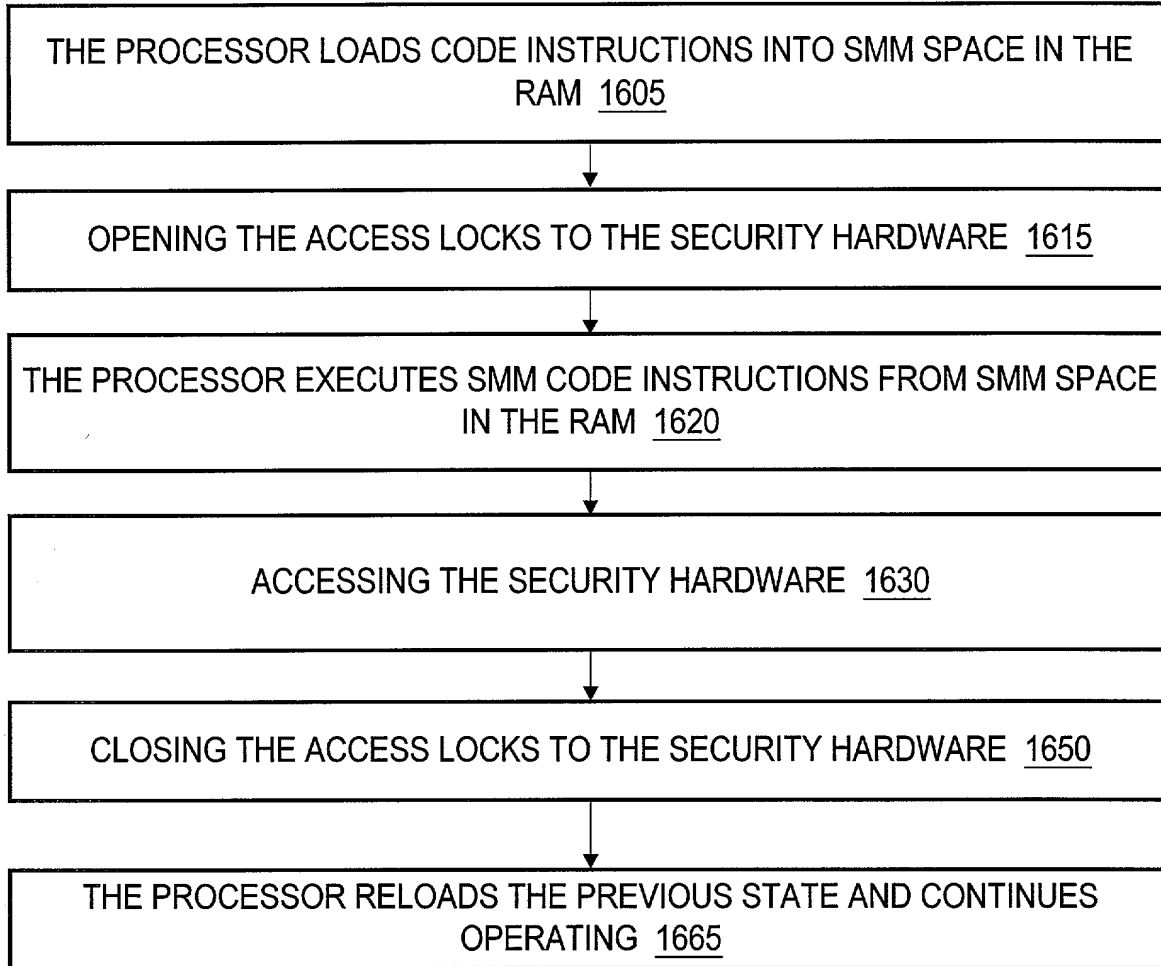


Fig. 16F

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1600G

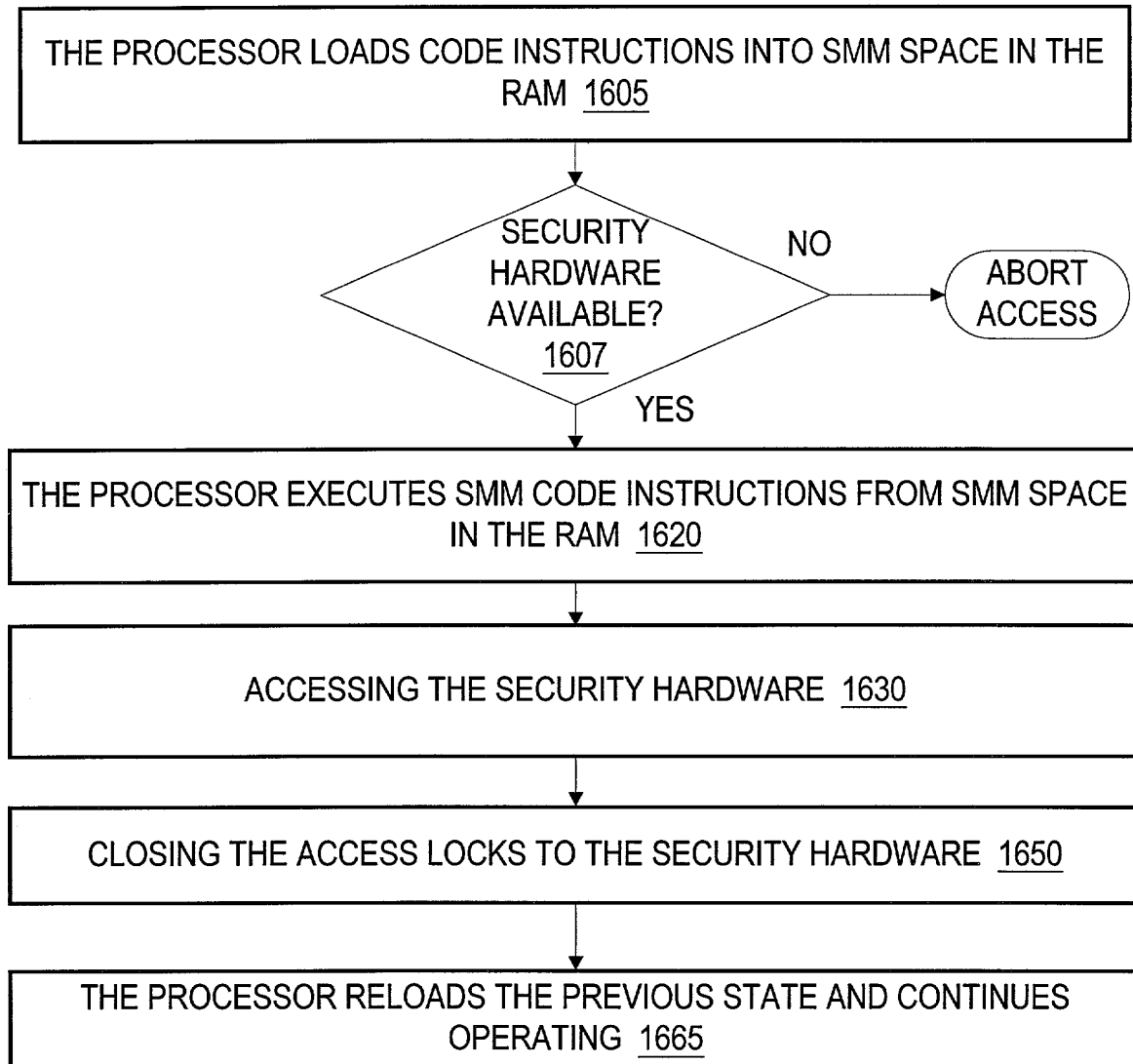


Fig. 16G

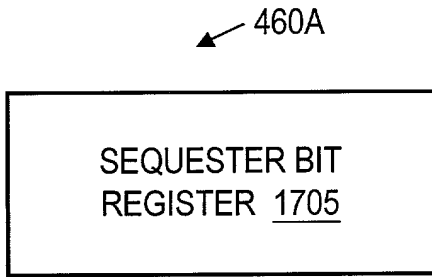


Fig. 17A

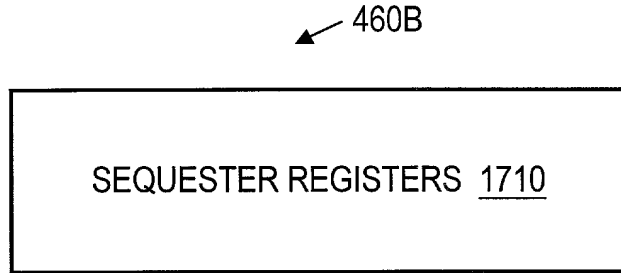


Fig. 17B

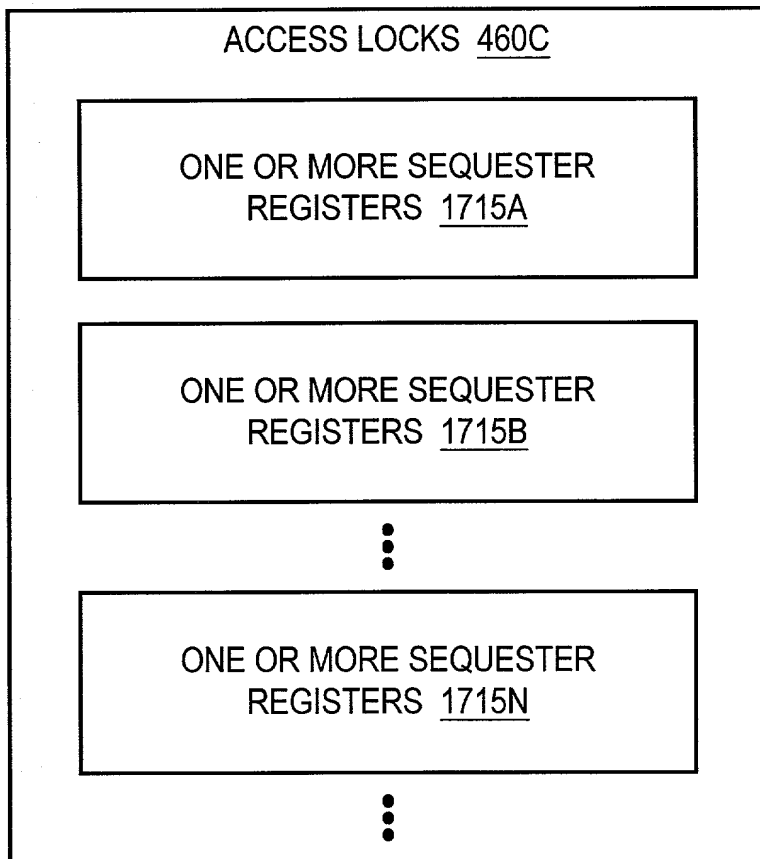


Fig. 17C

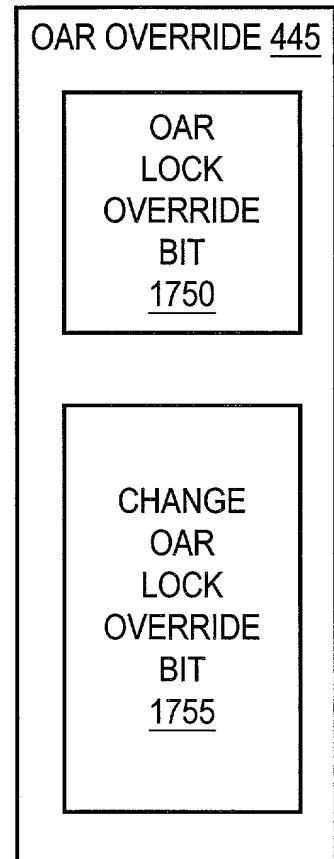


Fig. 17D

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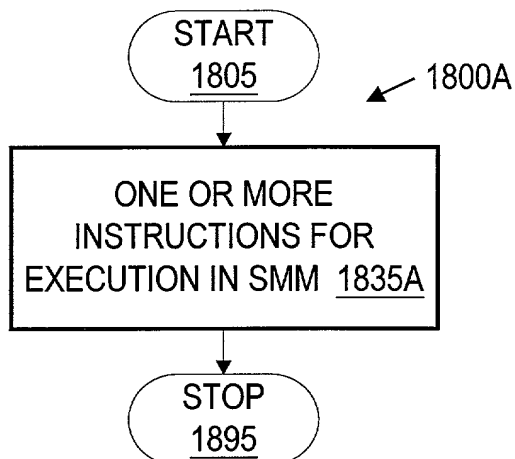


Fig. 18A
PRIOR ART

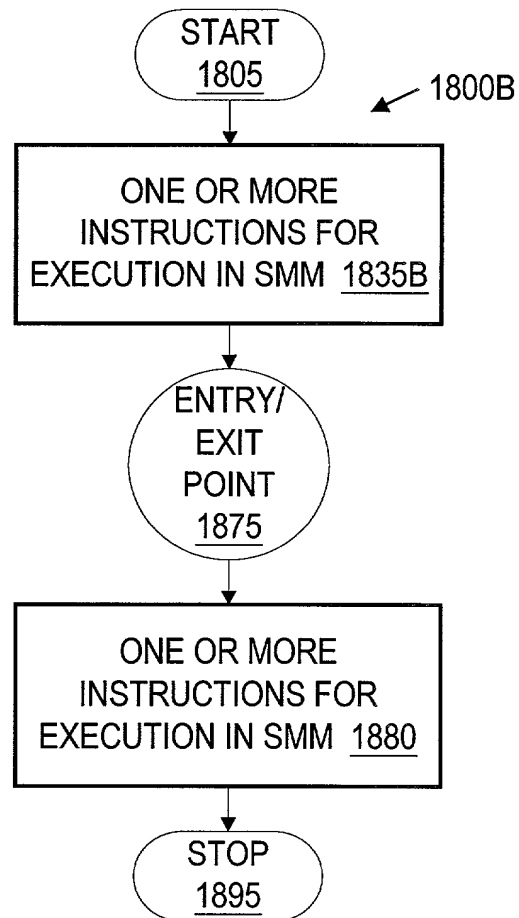


Fig. 18B

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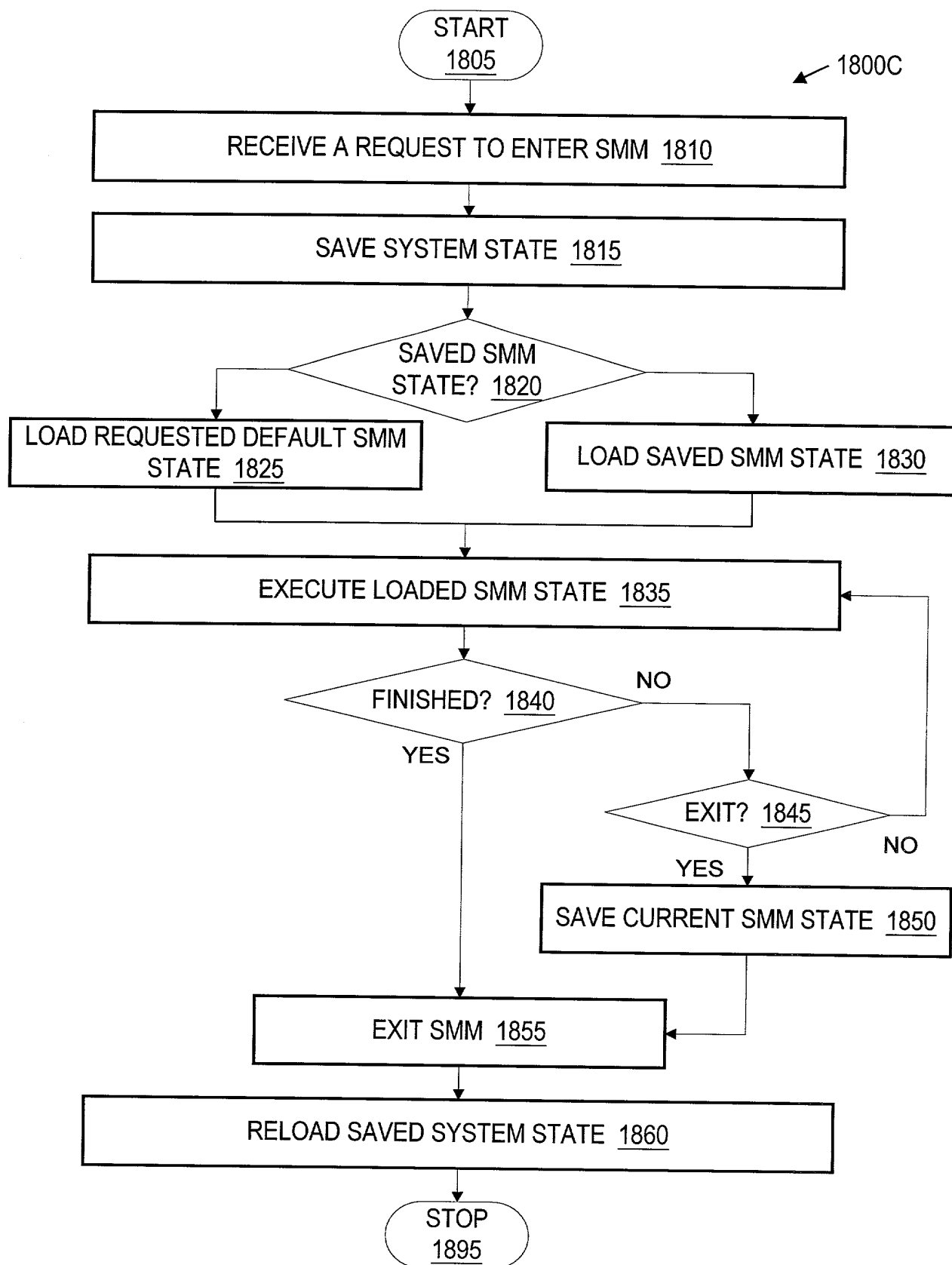


Fig. 18C

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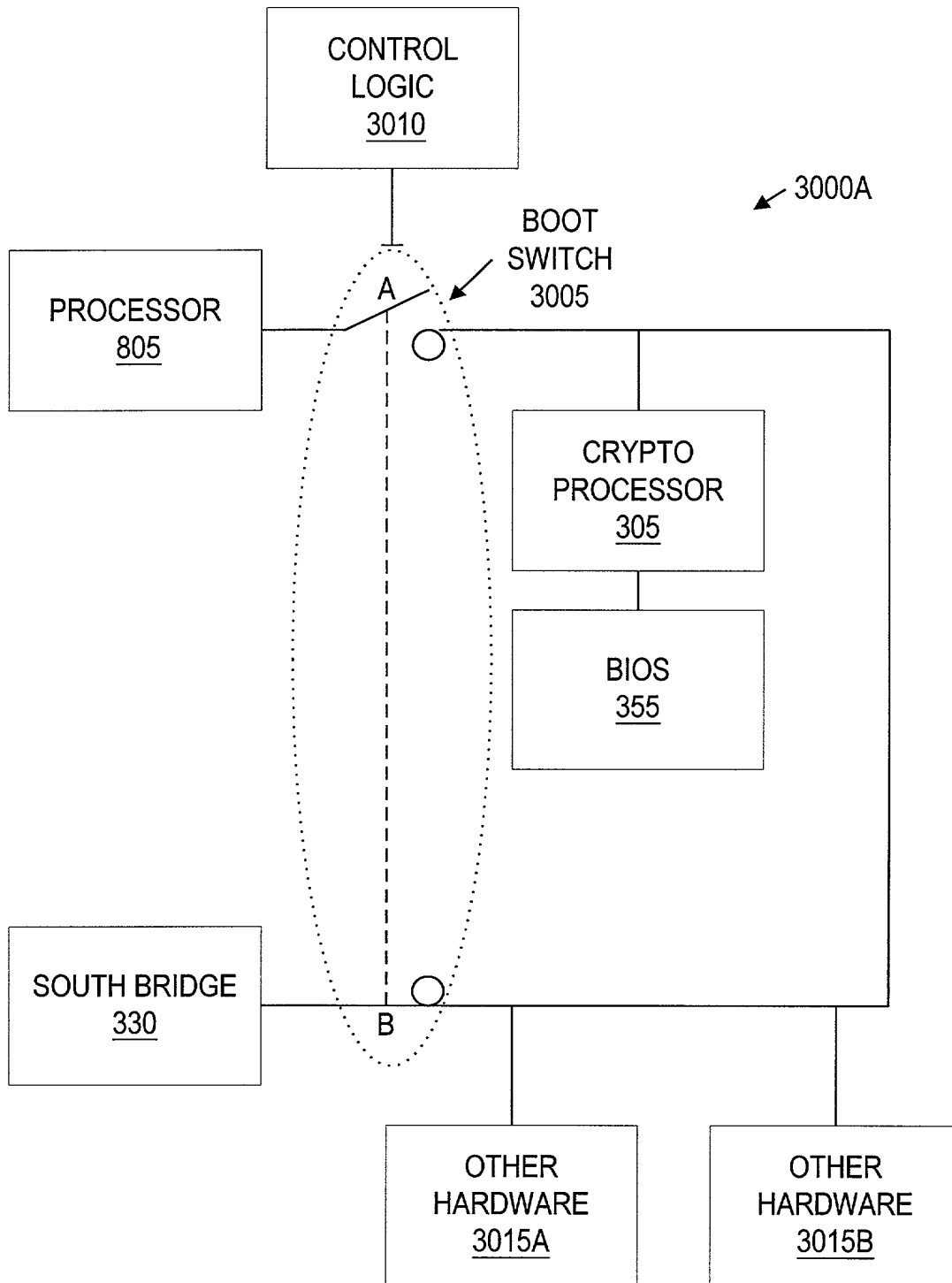


Fig. 19A

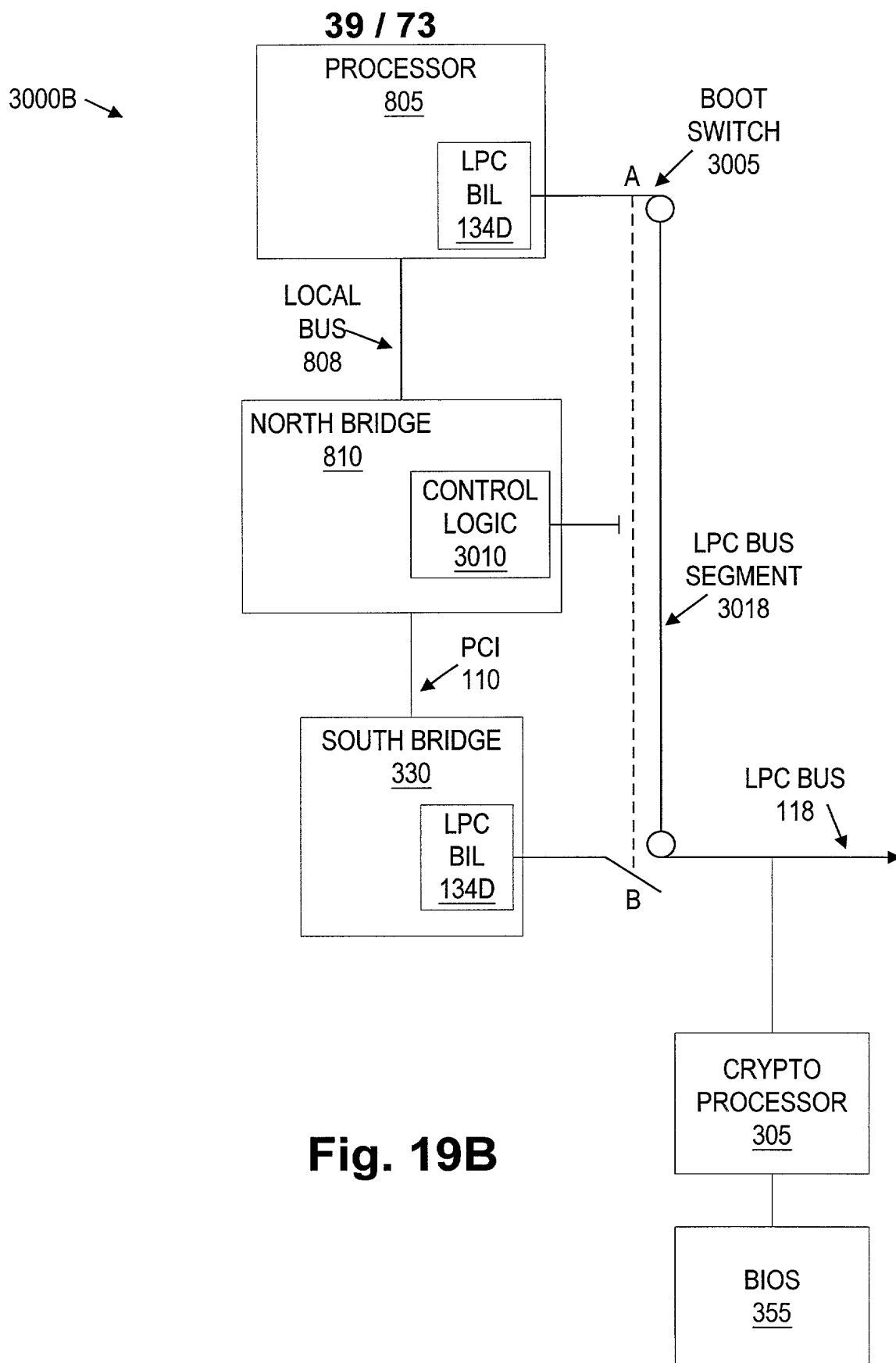


Fig. 19B

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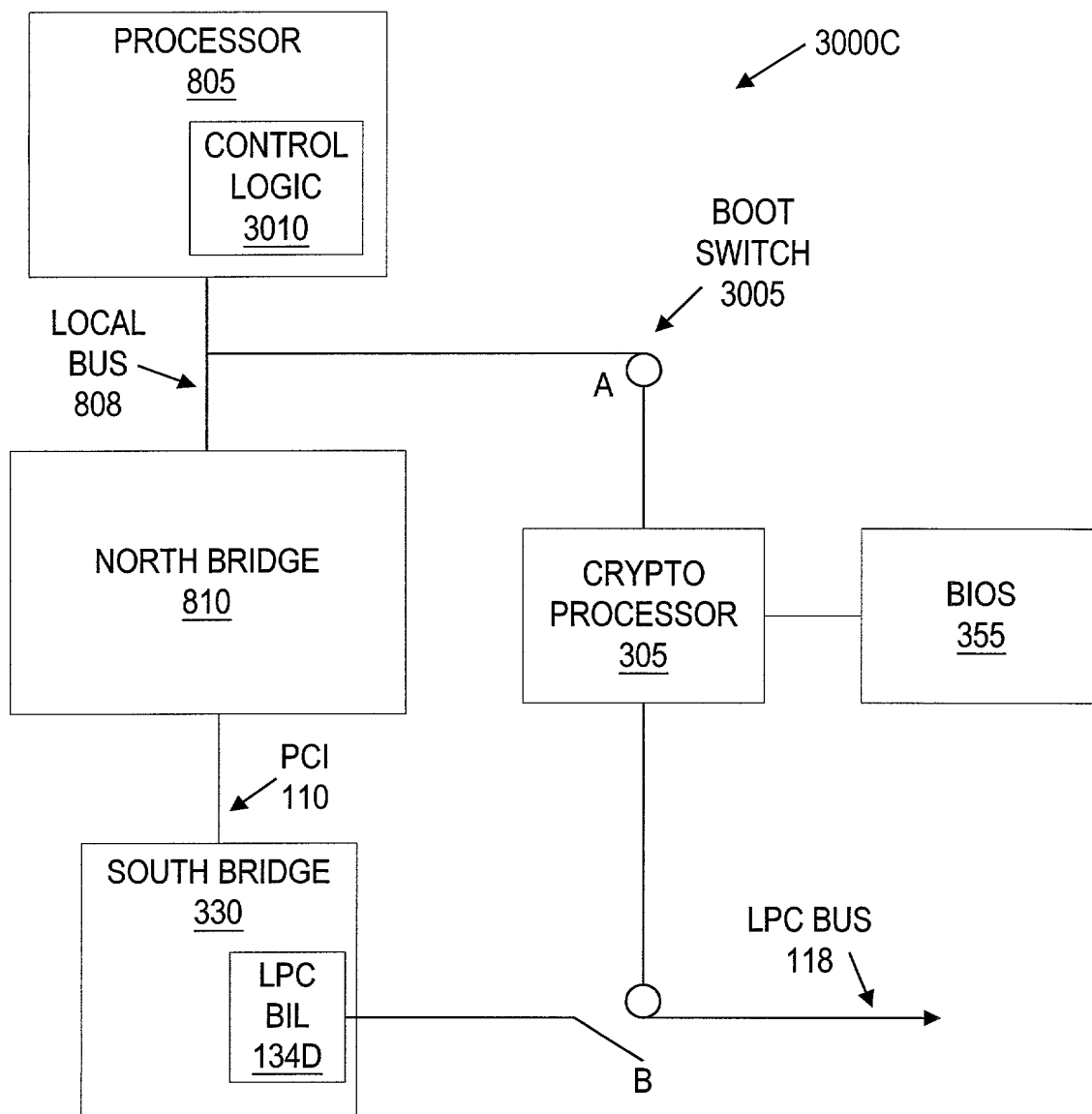


Fig. 19C

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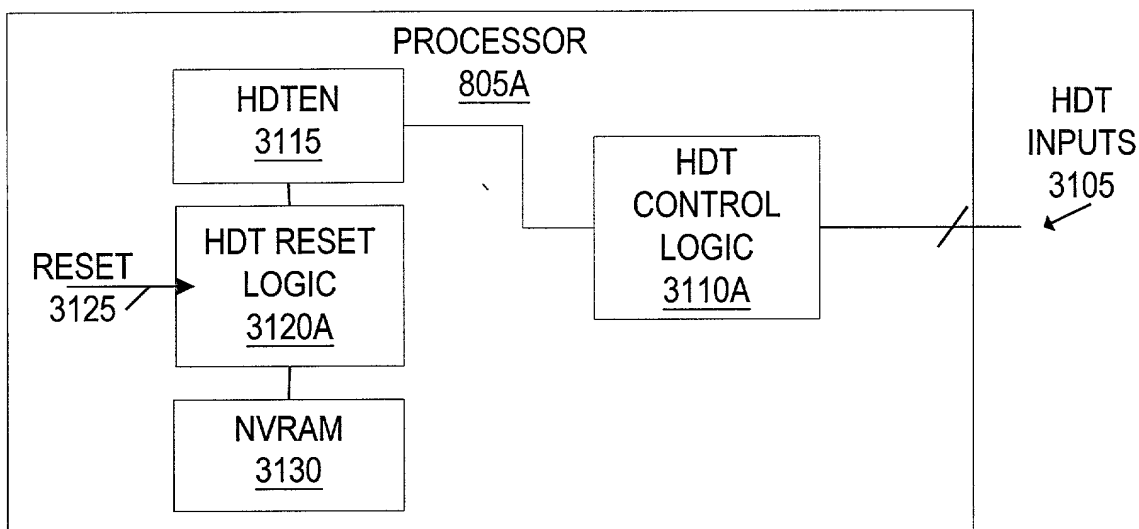


Fig. 20A

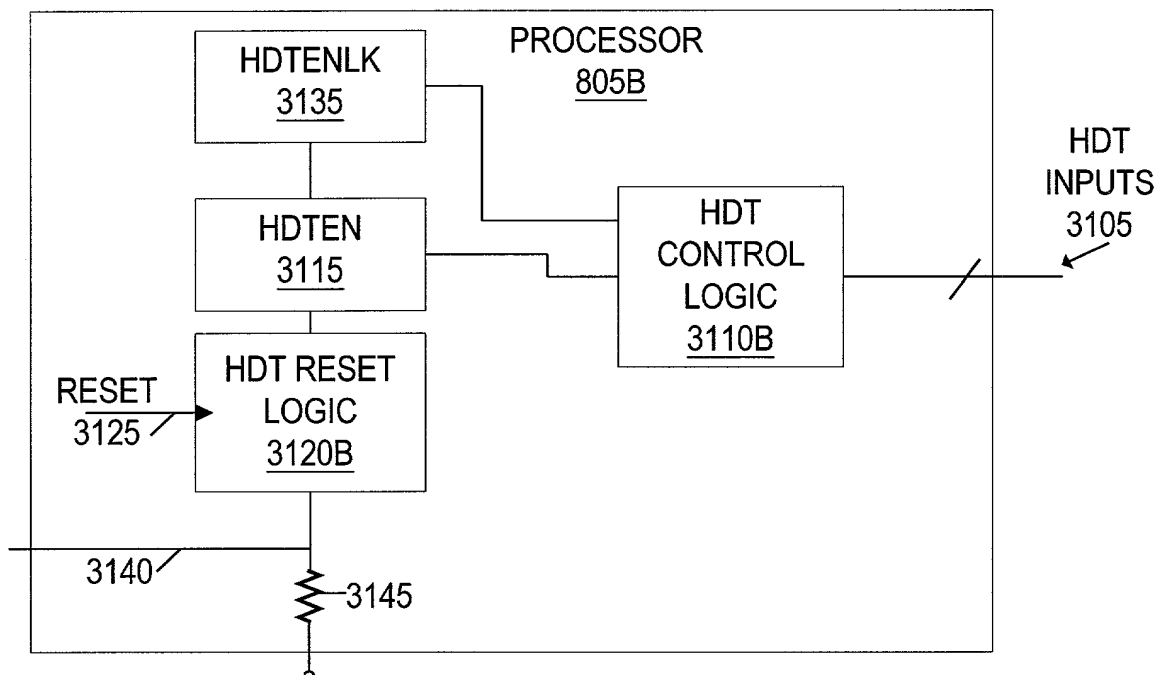


Fig. 20B

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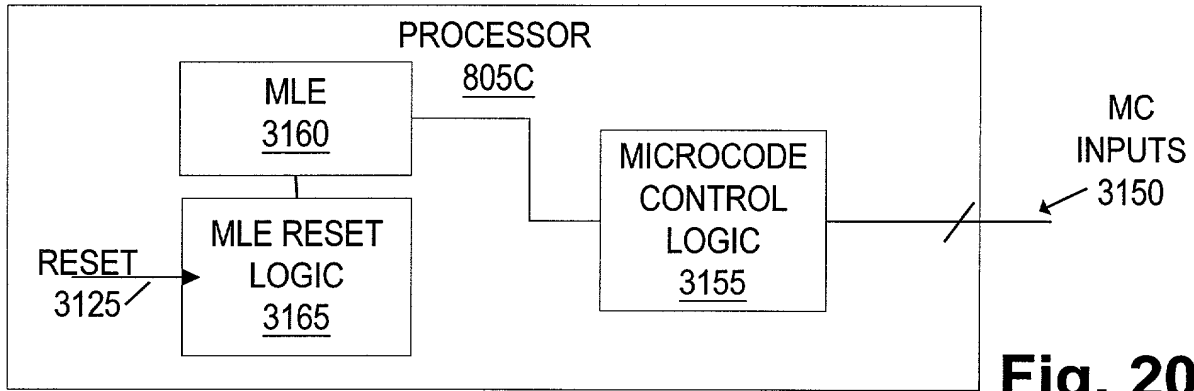


Fig. 20C

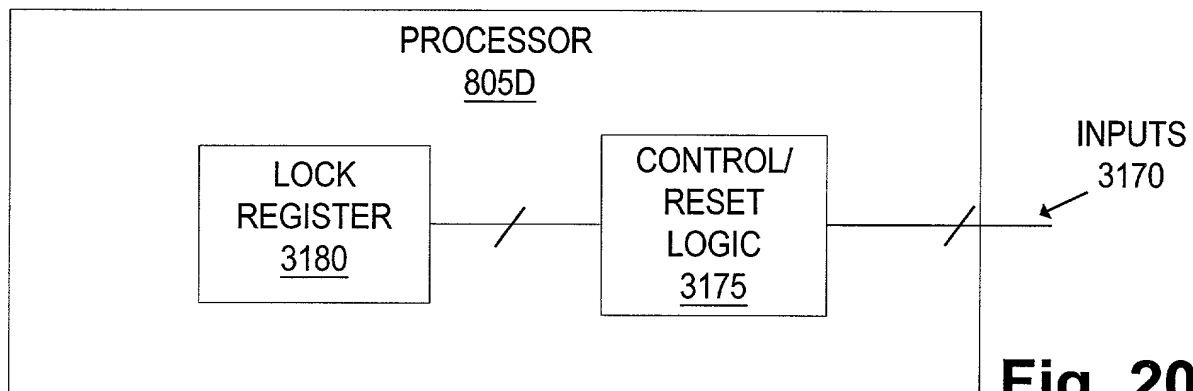


Fig. 20D

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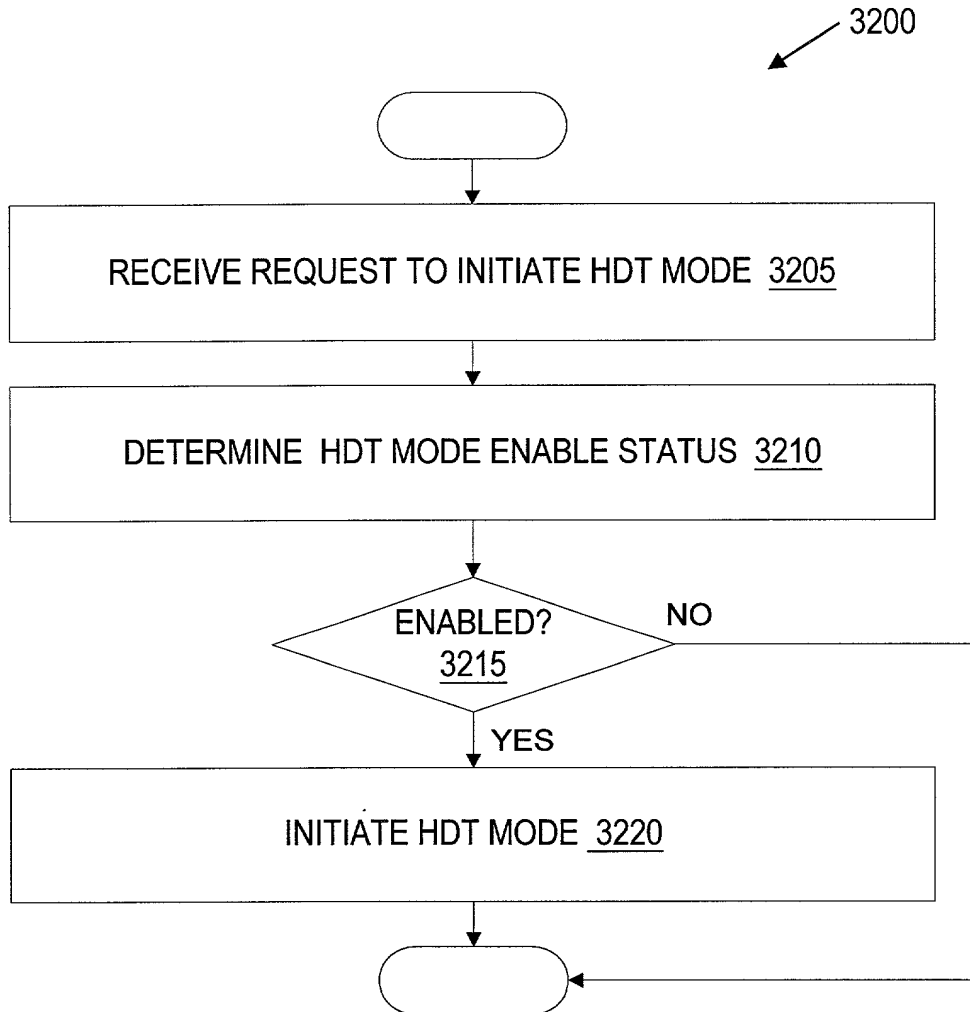


Fig. 21

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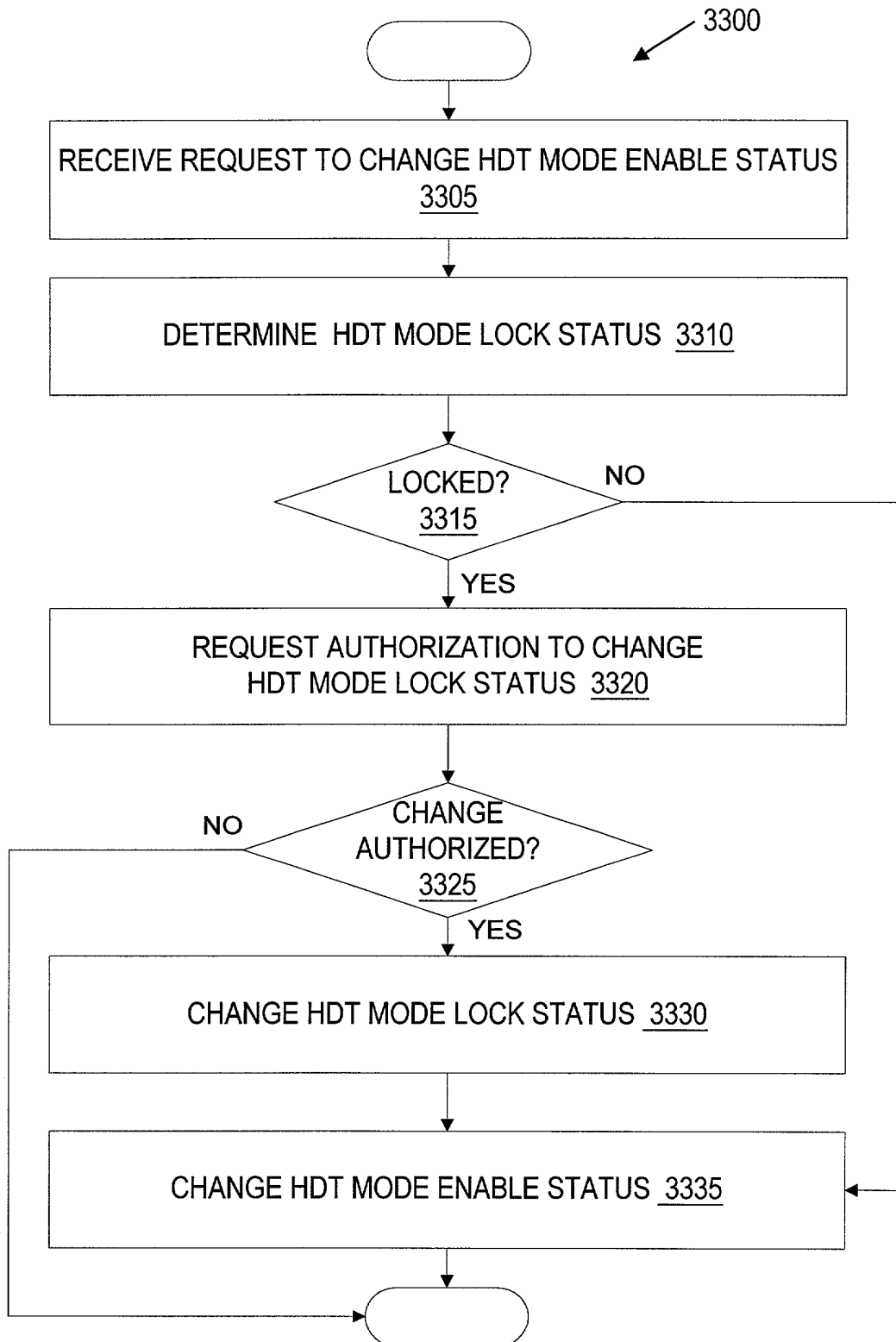


Fig. 22

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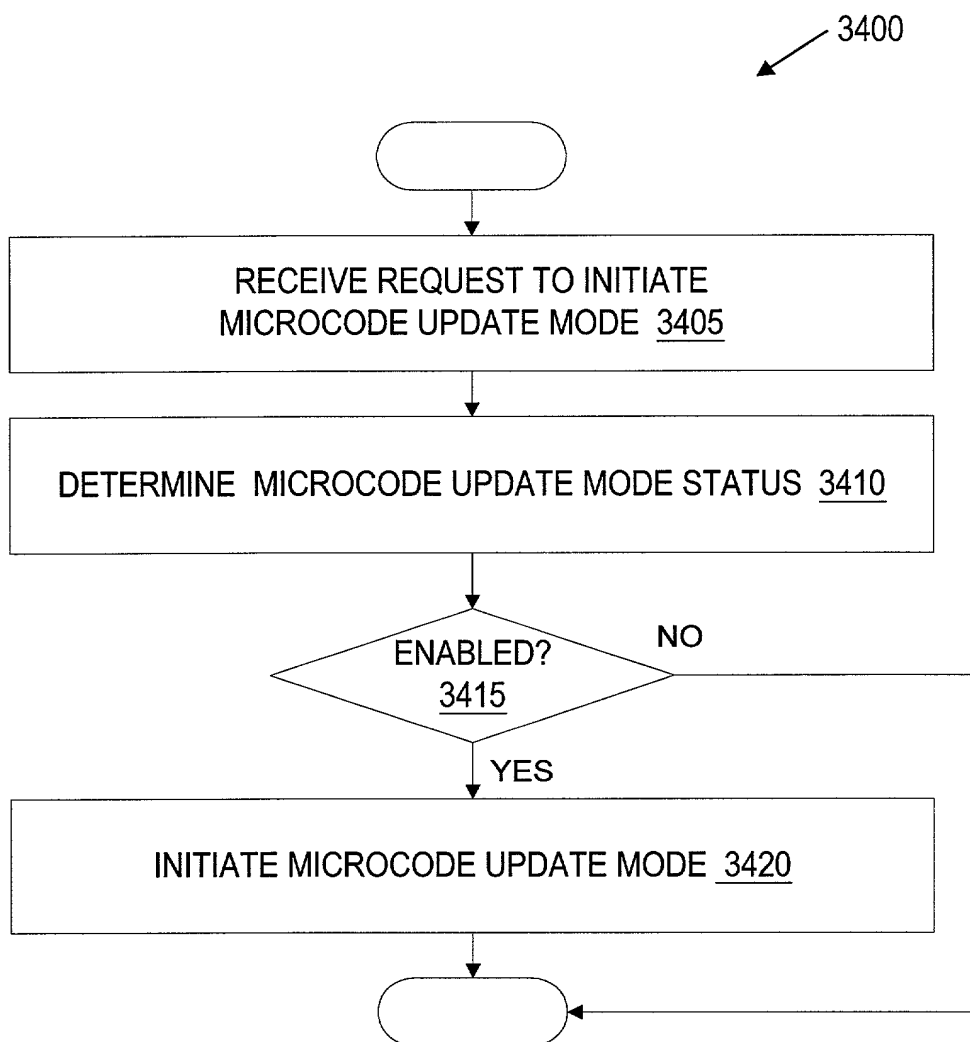


Fig. 23

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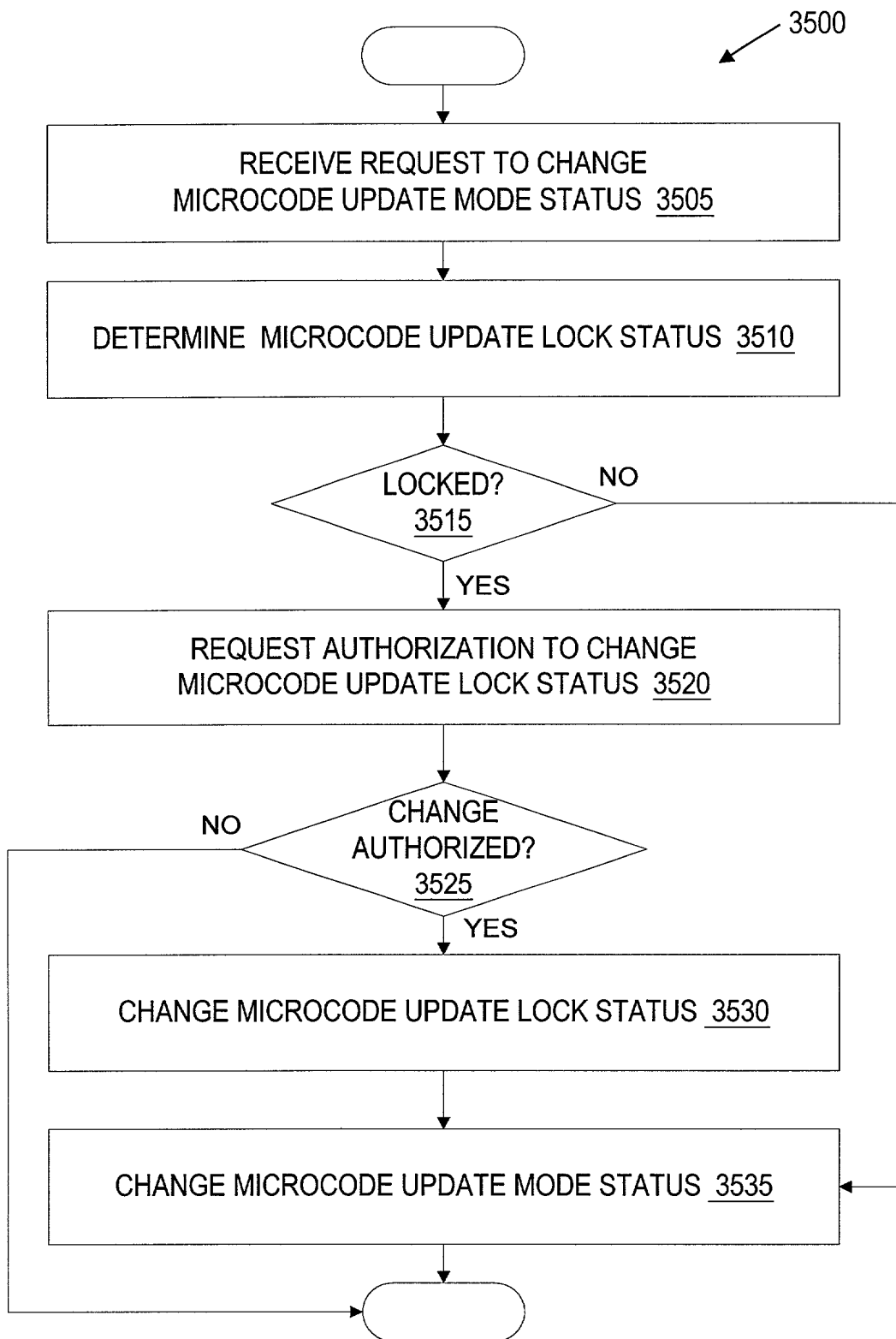


Fig. 24

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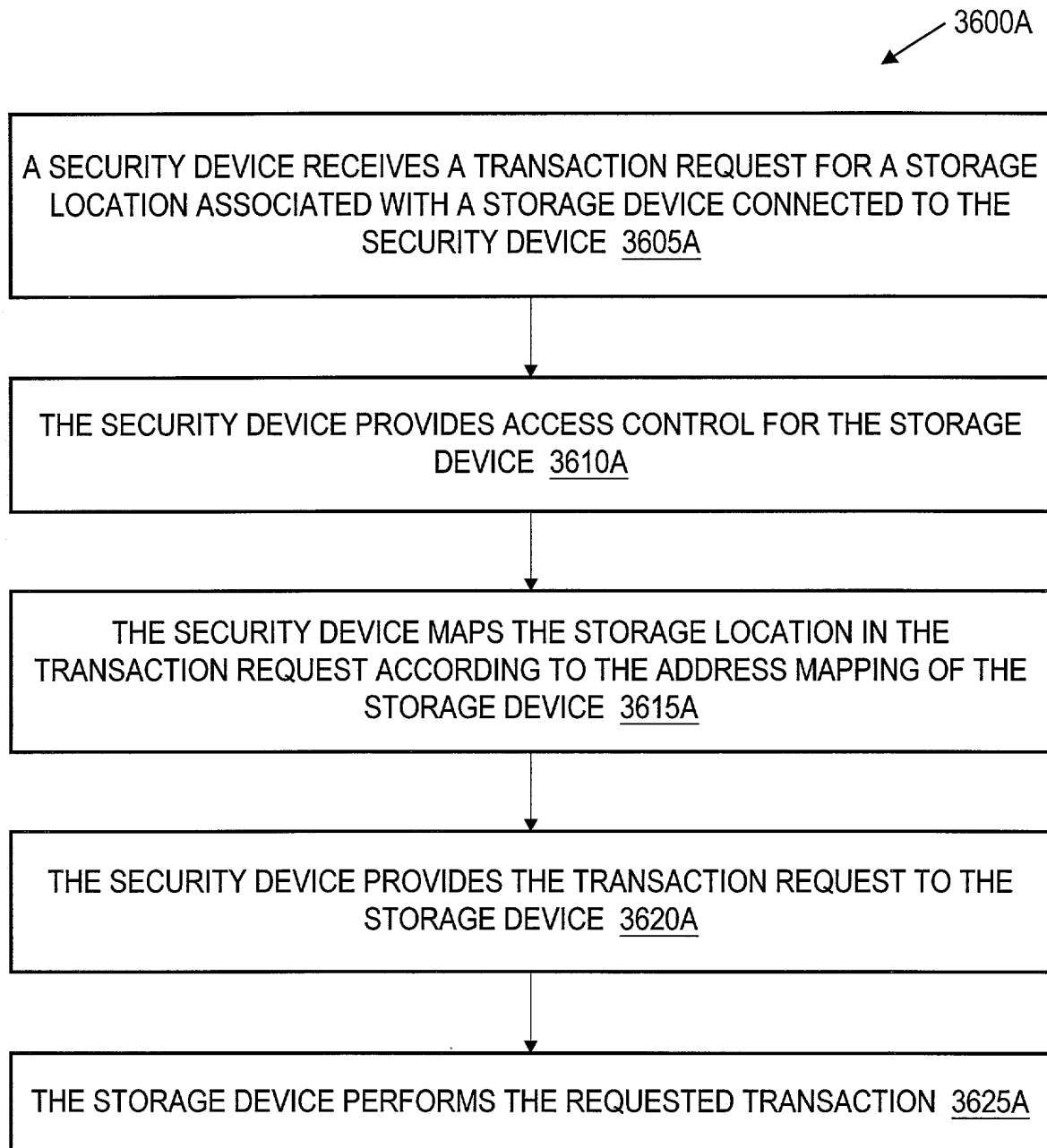


Fig. 25A

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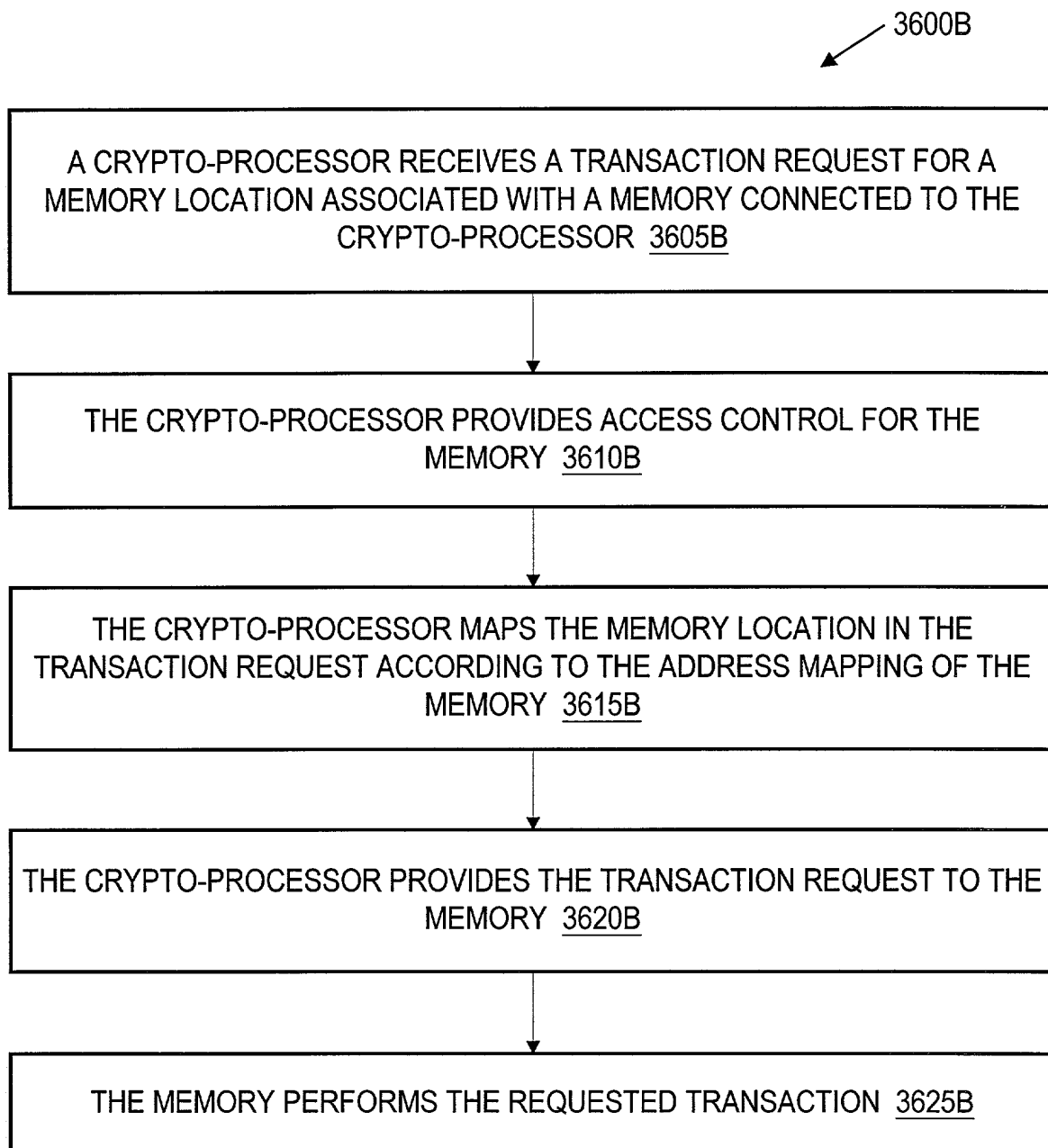


Fig. 25B

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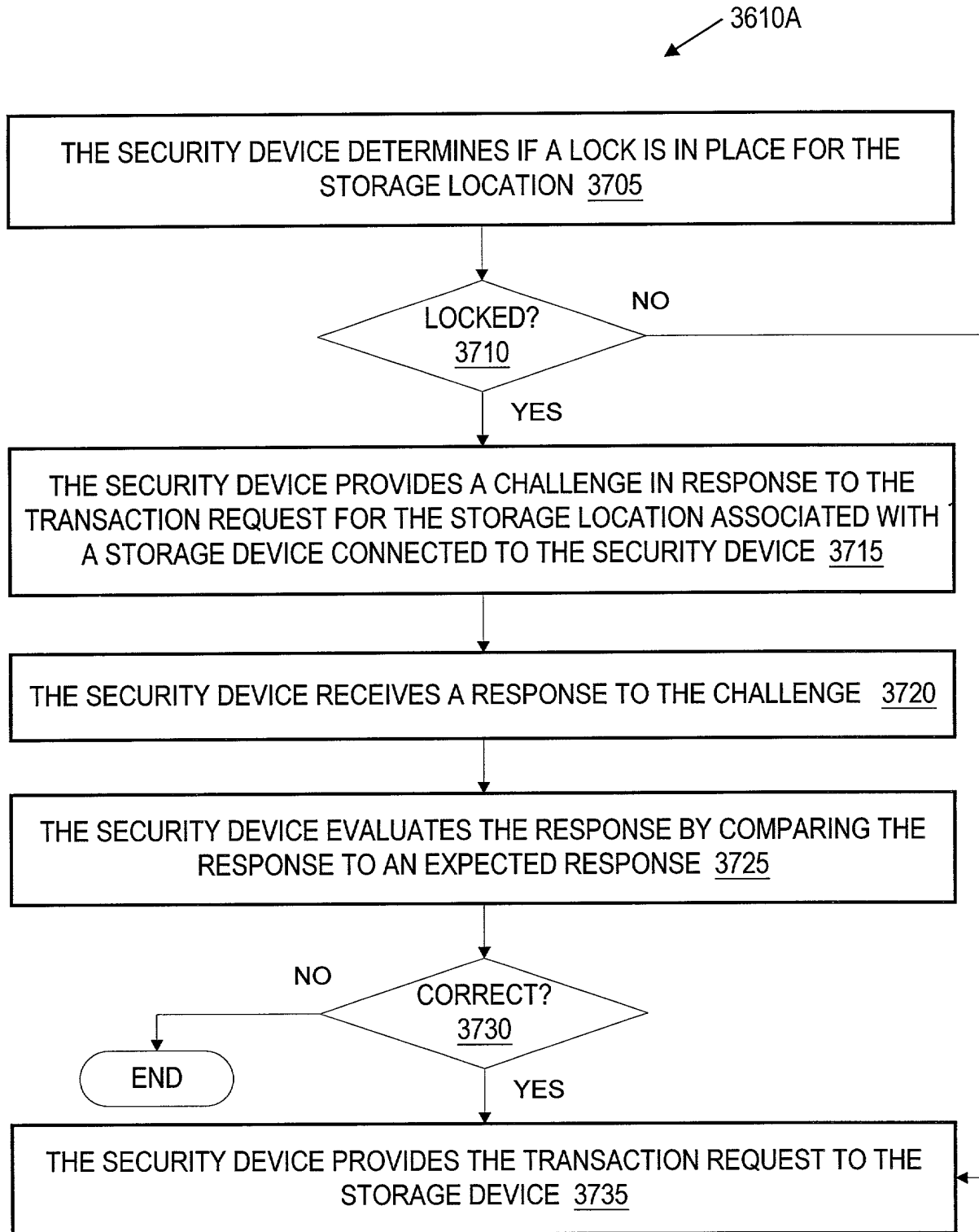


Fig. 26

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3620

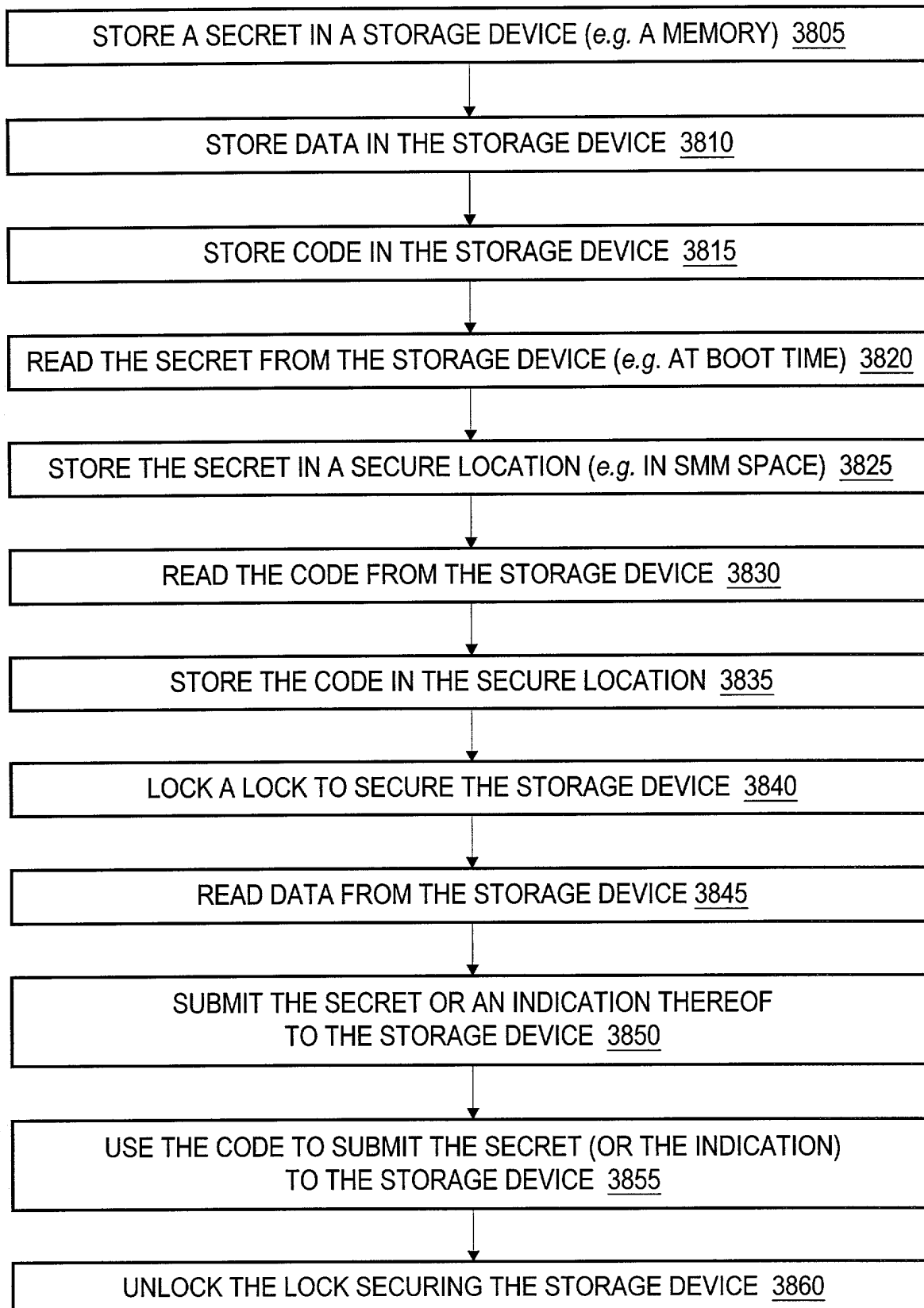


Fig. 27

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3900

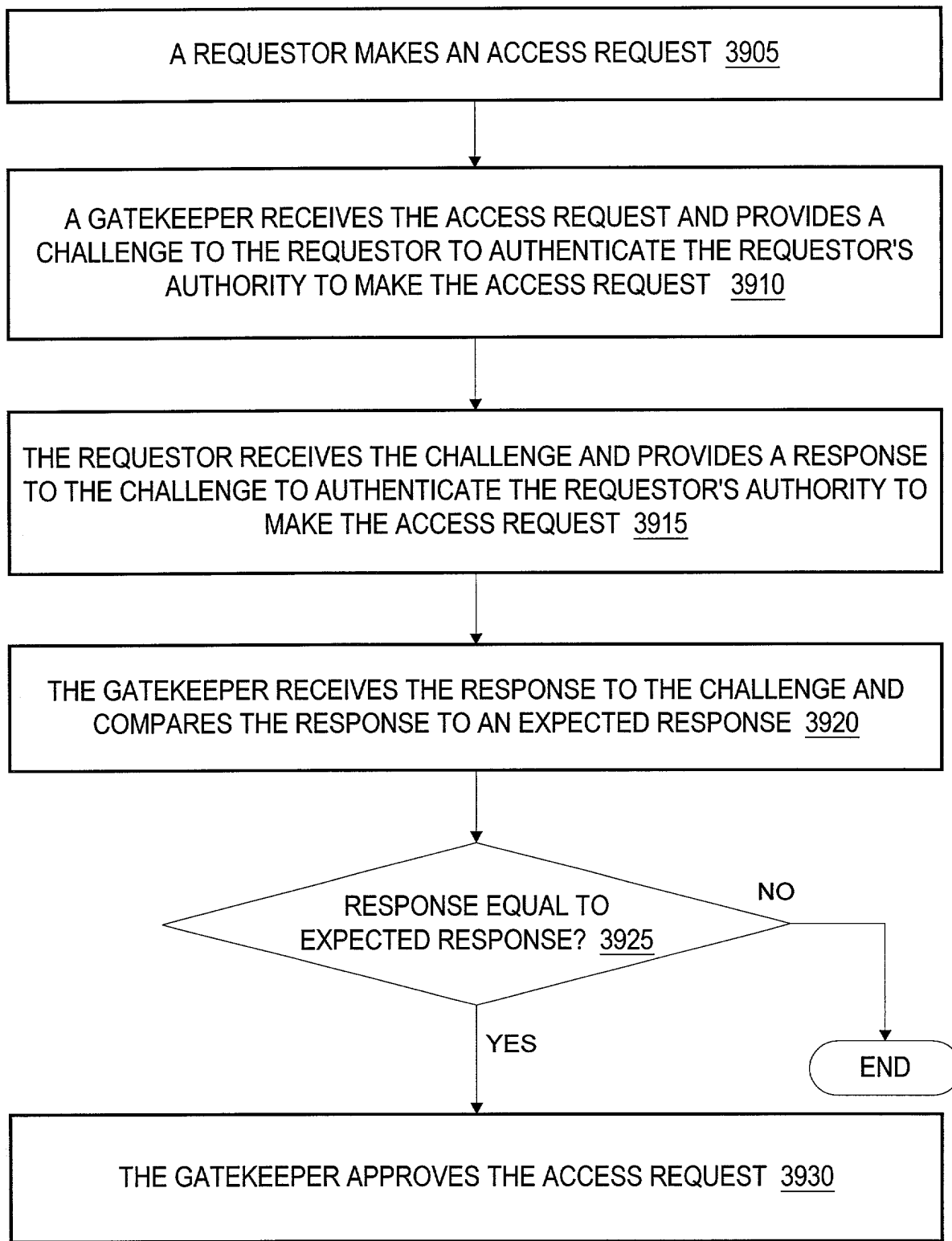


Fig. 28
(Prior Art)

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4000A

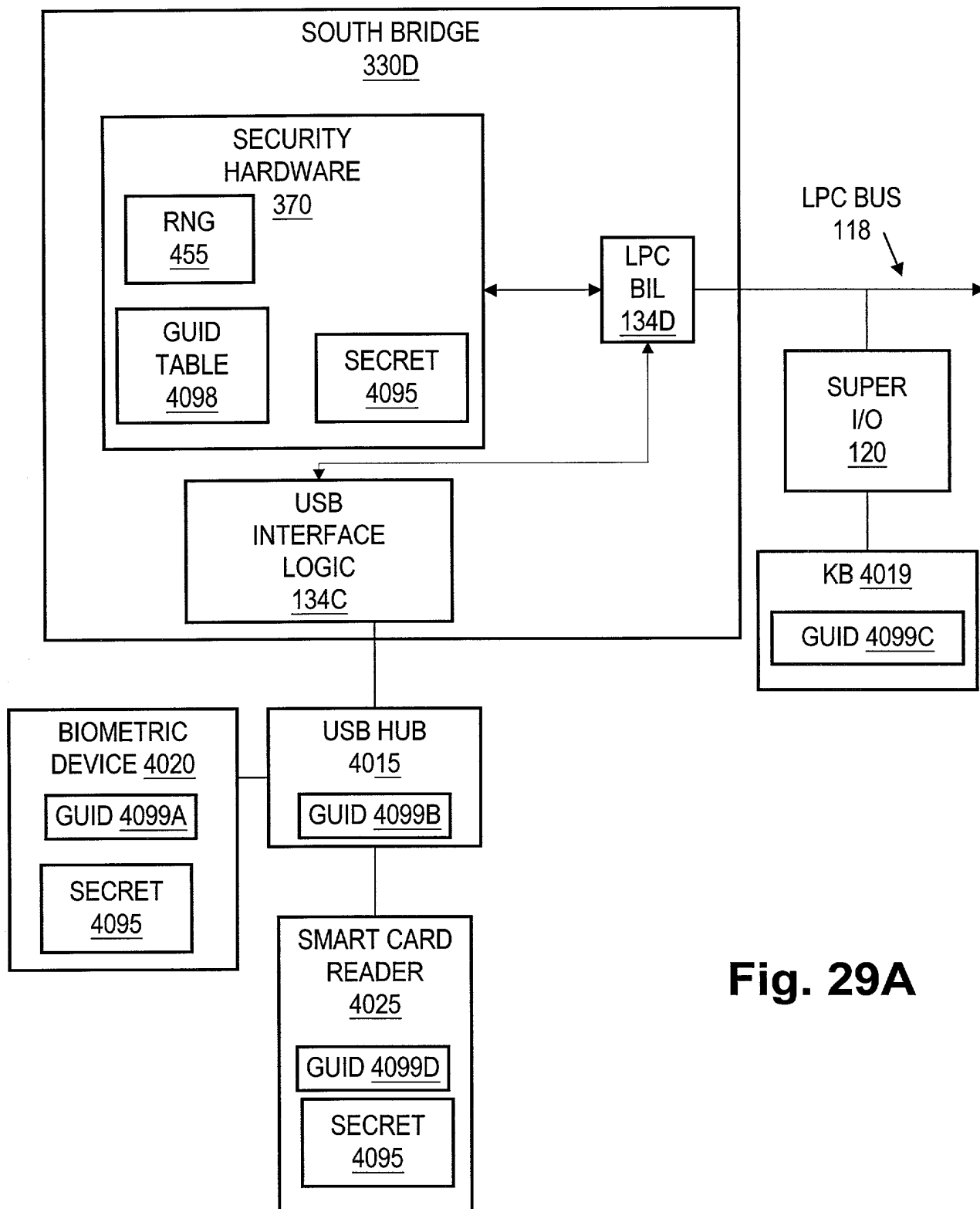


Fig. 29A



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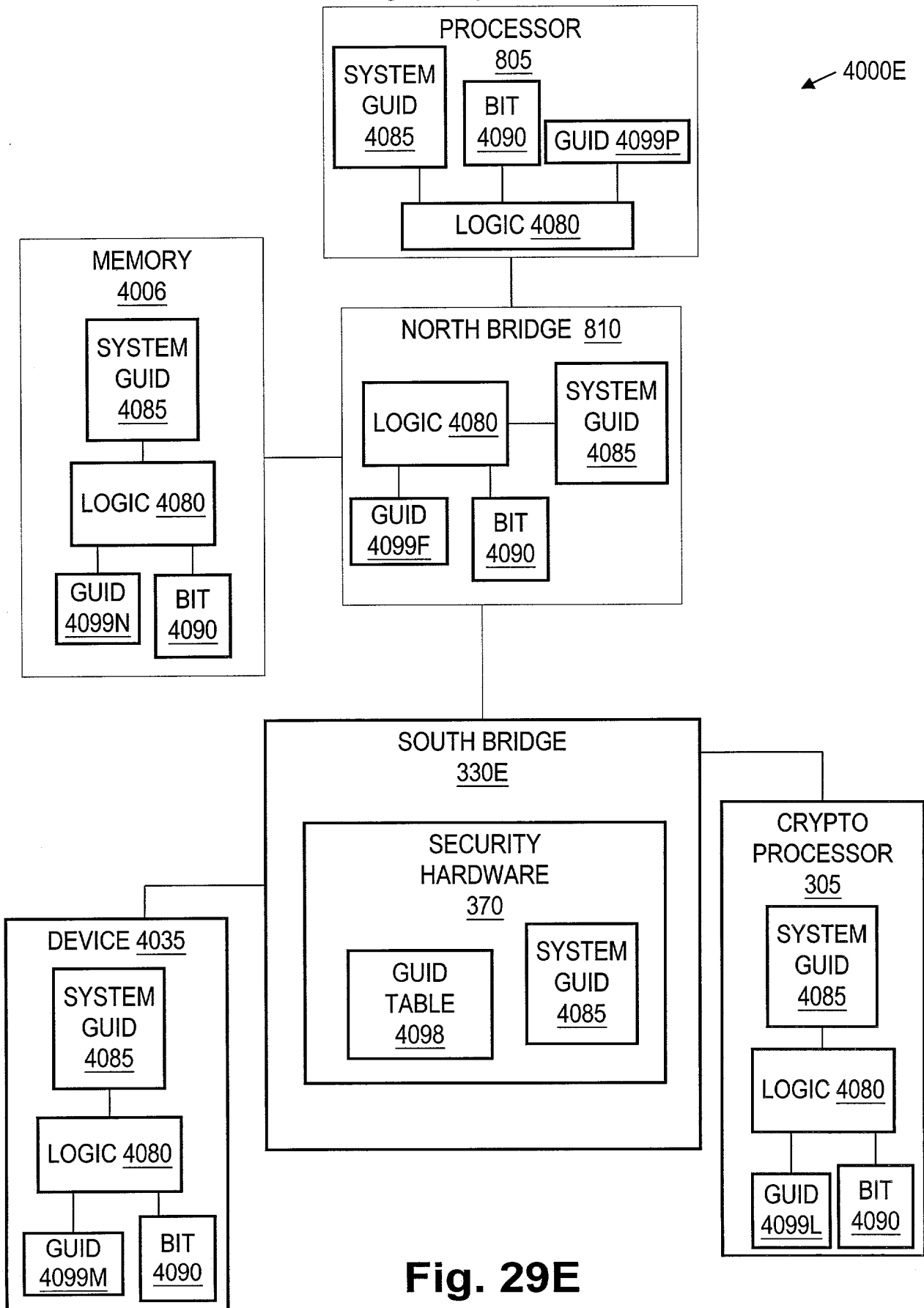


Fig. 29E

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4100A

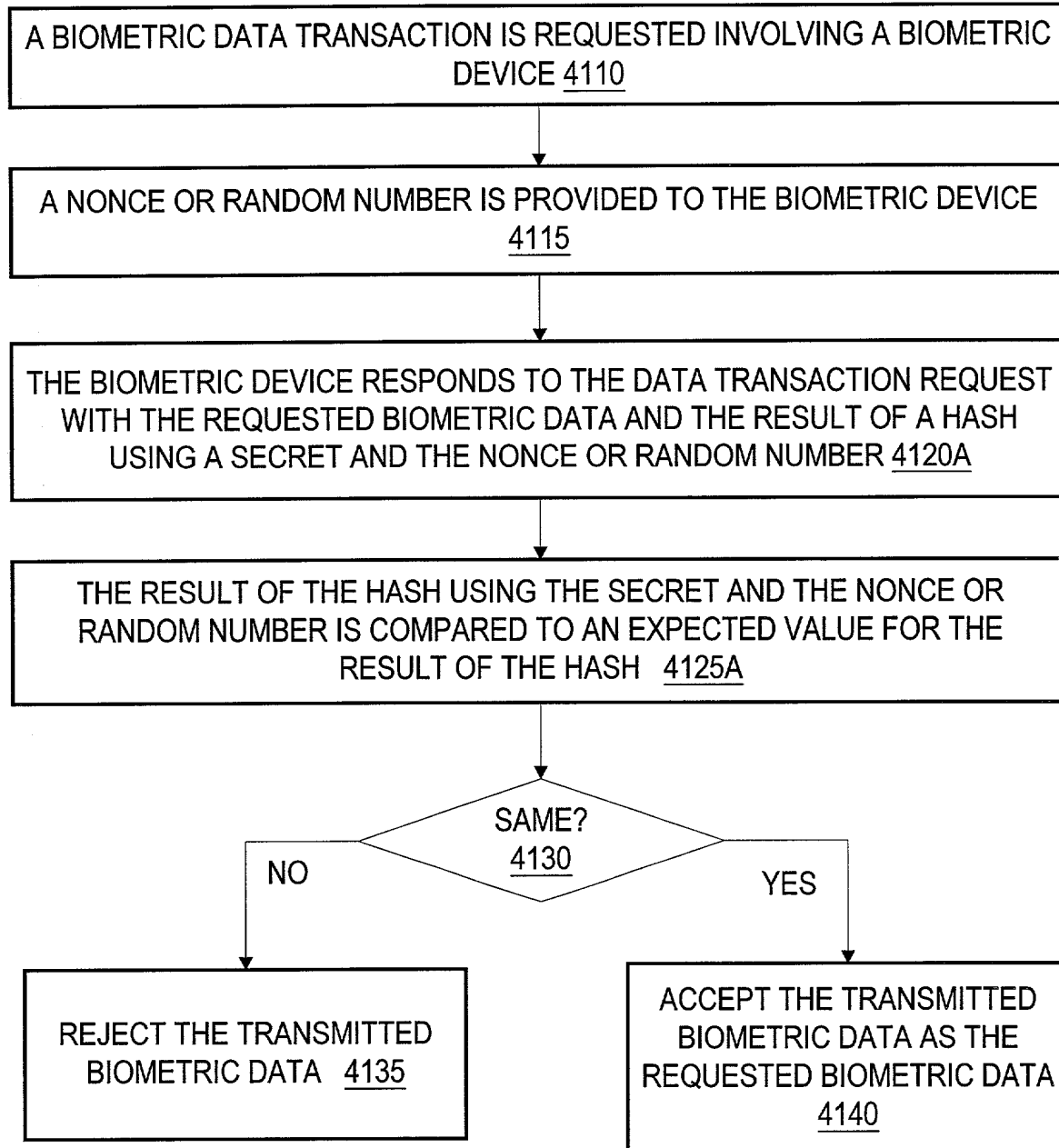


Fig. 30A

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4100B

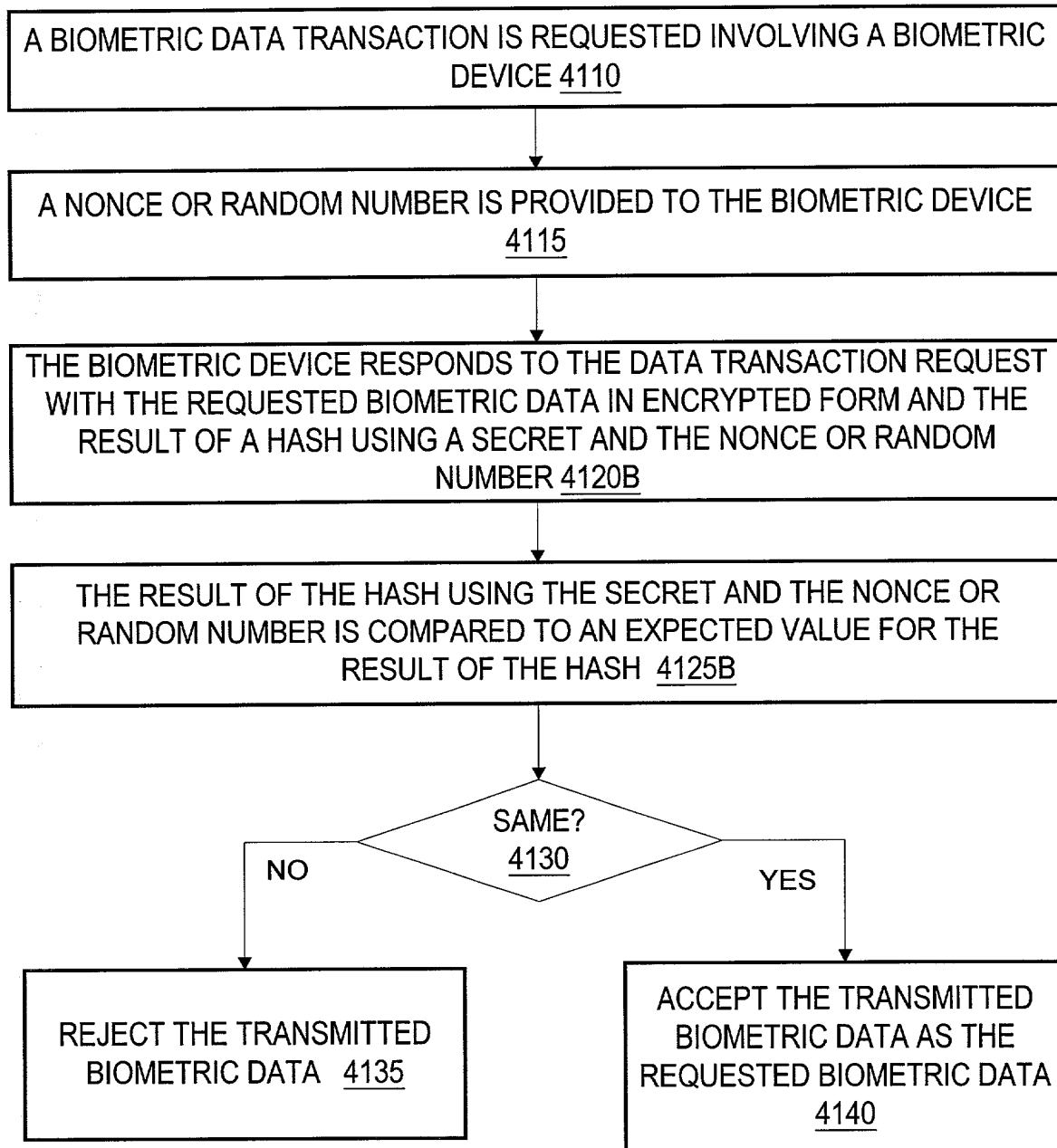


Fig. 30B

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4200A

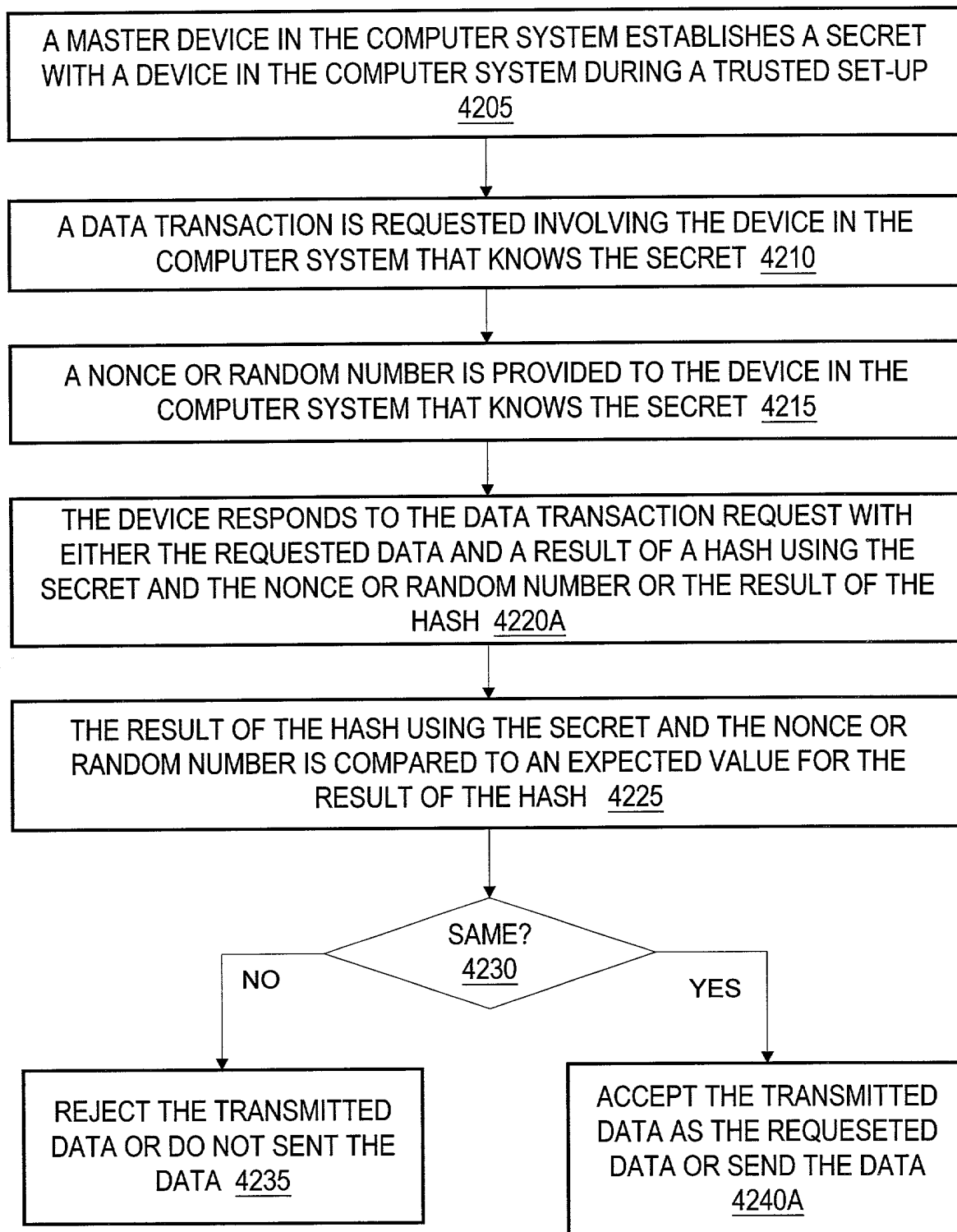
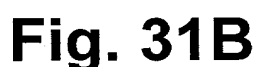


Fig. 31A



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4300A

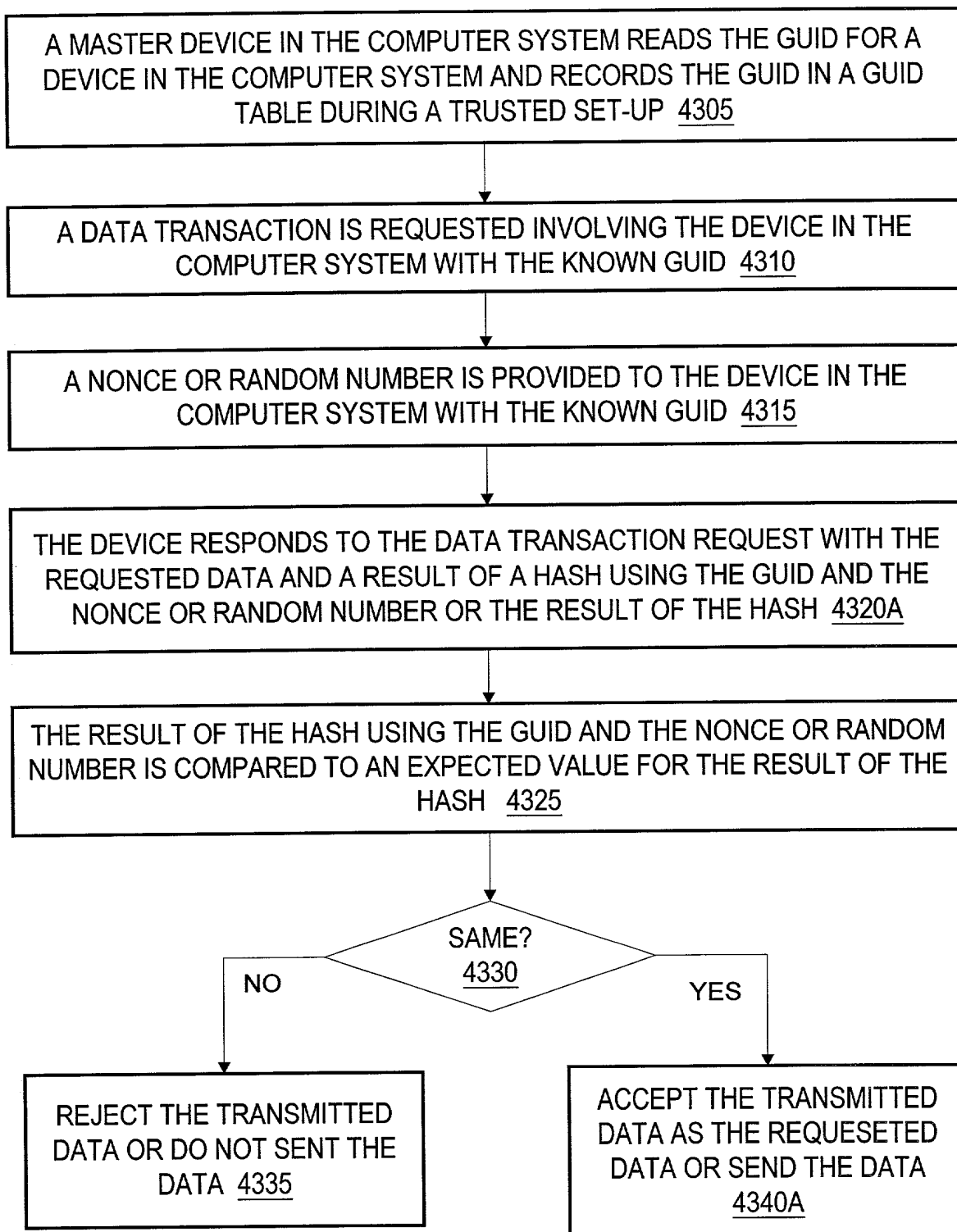


Fig. 32A

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4300B

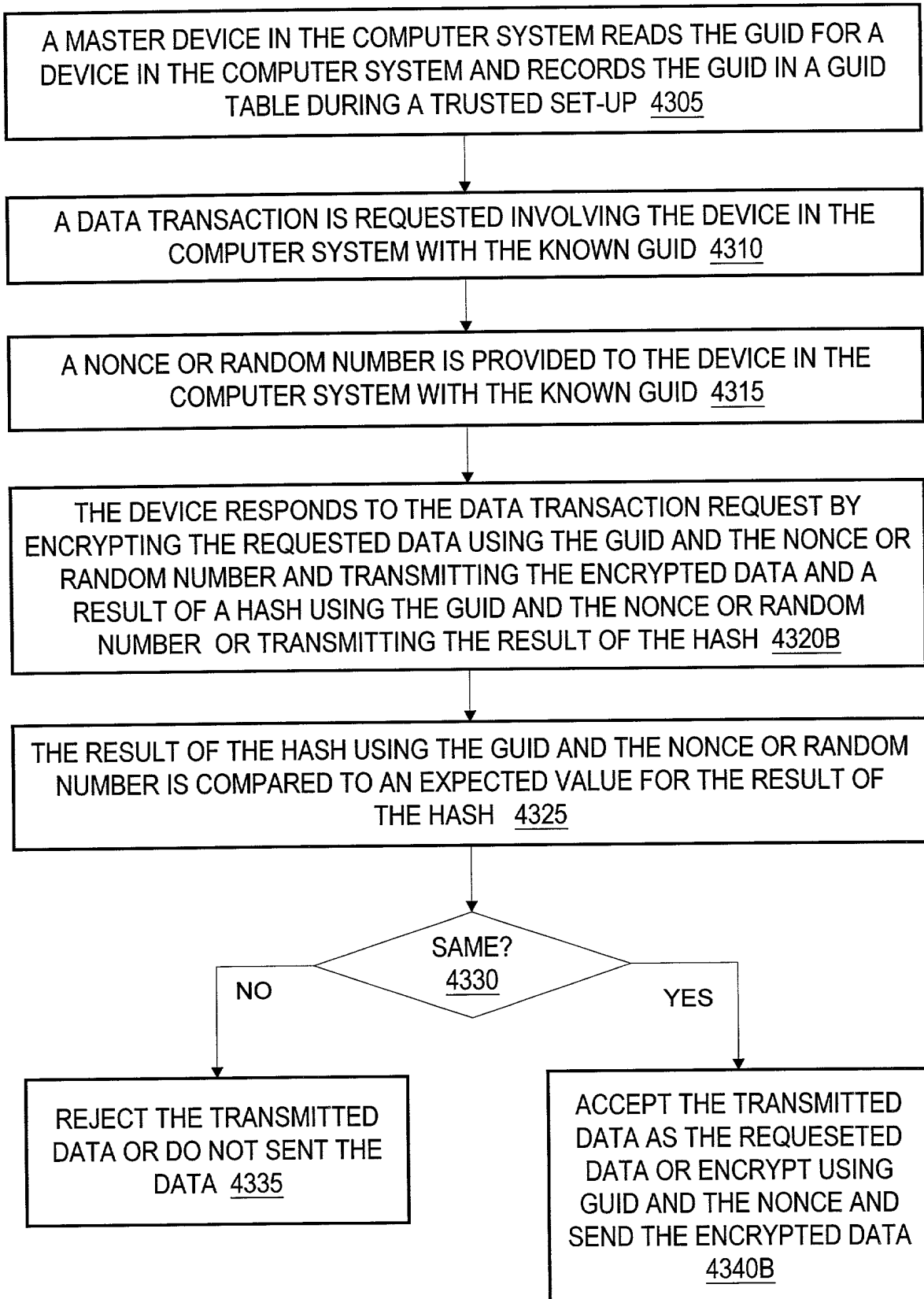


Fig. 32B

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4300C

A MASTER DEVICE IN THE COMPUTER SYSTEM READS THE GUID FOR A DEVICE IN THE COMPUTER SYSTEM, RECORDS THE GUID IN A GUID TABLE, AND TRANSMITS A SECRET TO THE DEVICE DURING A TRUSTED SET-UP

4306

A DATA TRANSACTION IS REQUESTED INVOLVING THE DEVICE IN THE COMPUTER SYSTEM WITH THE KNOWN GUID THAT KNOWS THE SECRET

4311

A NONCE OR RANDOM NUMBER IS PROVIDED TO THE DEVICE IN THE COMPUTER SYSTEM WITH THE KNOWN GUID THAT KNOWS THE SECRET

4316

THE DEVICE RESPONDS TO THE DATA TRANSACTION REQUEST BY ENCRYPTING THE REQUESTED DATA USING THE SECRET, THE GUID, AND THE NONCE OR RANDOM NUMBER AND TRANSMITTING THE ENCRYPTED DATA AND A RESULT OF A HASH USING THE SECRET, THE GUID, AND THE NONCE OR RANDOM NUMBER OR TRANSMITTING THE RESULT OF THE HASH 4320C

THE RESULT OF THE HASH USING THE SECRET, THE GUID, AND THE NONCE OR RANDOM NUMBER IS COMPARED TO AN EXPECTED VALUE FOR THE RESULT OF THE HASH 4326

SAME?

4330

NO

YES

REJECT THE TRANSMITTED DATA OR DO NOT SENT THE DATA 4335

ACCEPT THE TRANSMITTED DATA AS THE REQUESETED DATA OR ENCRYPT USING THE SECRET, THE GUID, AND THE NONCE AND SEND THE ENCRYPTED DATA 4340C

Fig. 32C

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4400

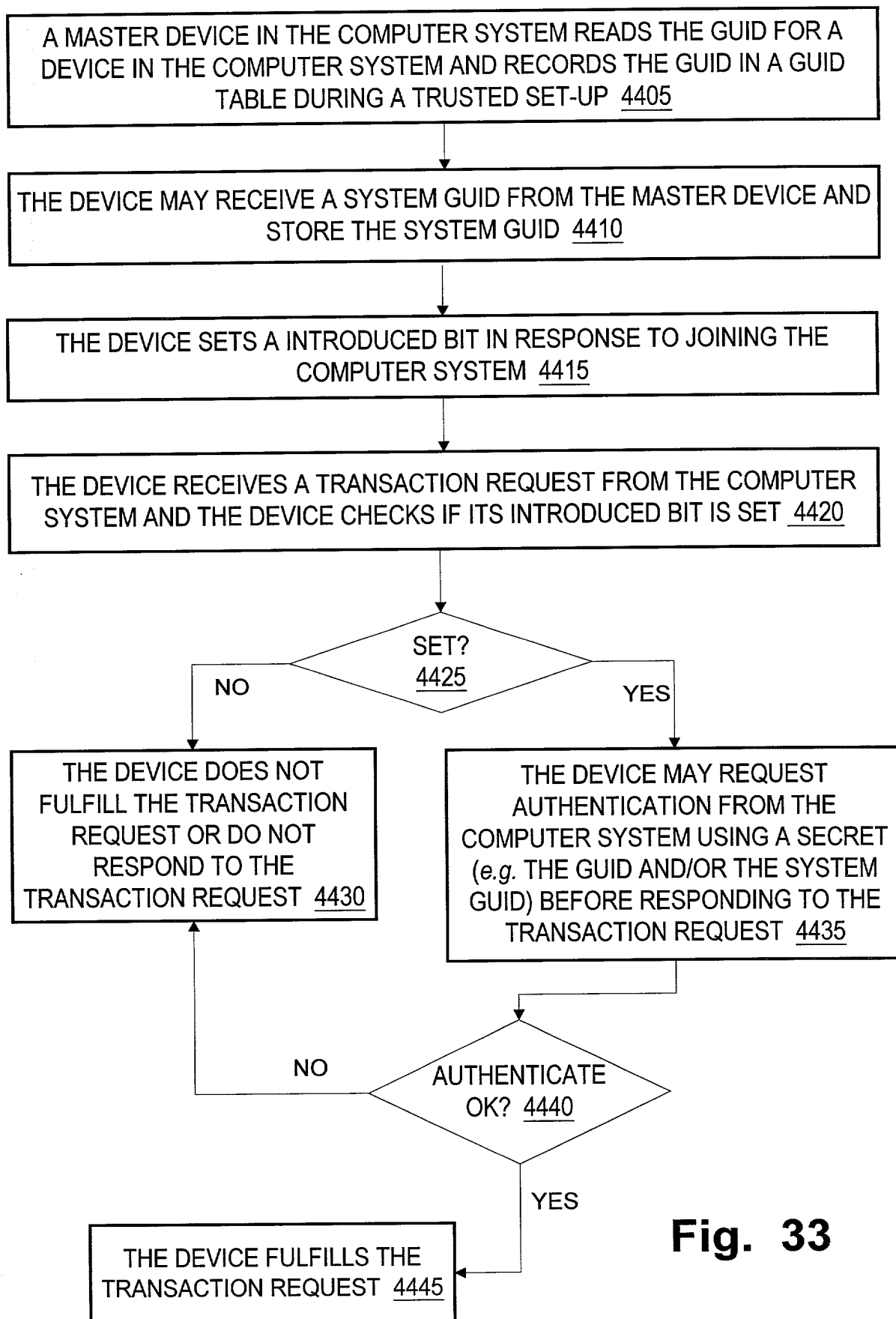


Fig. 33

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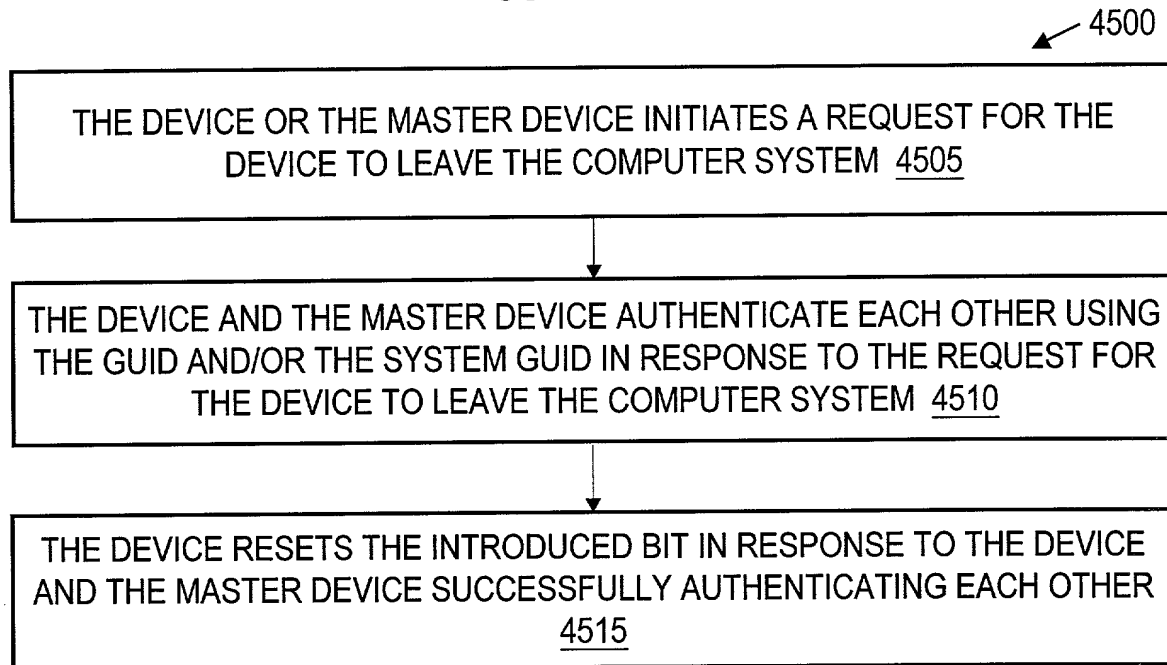


Fig. 34

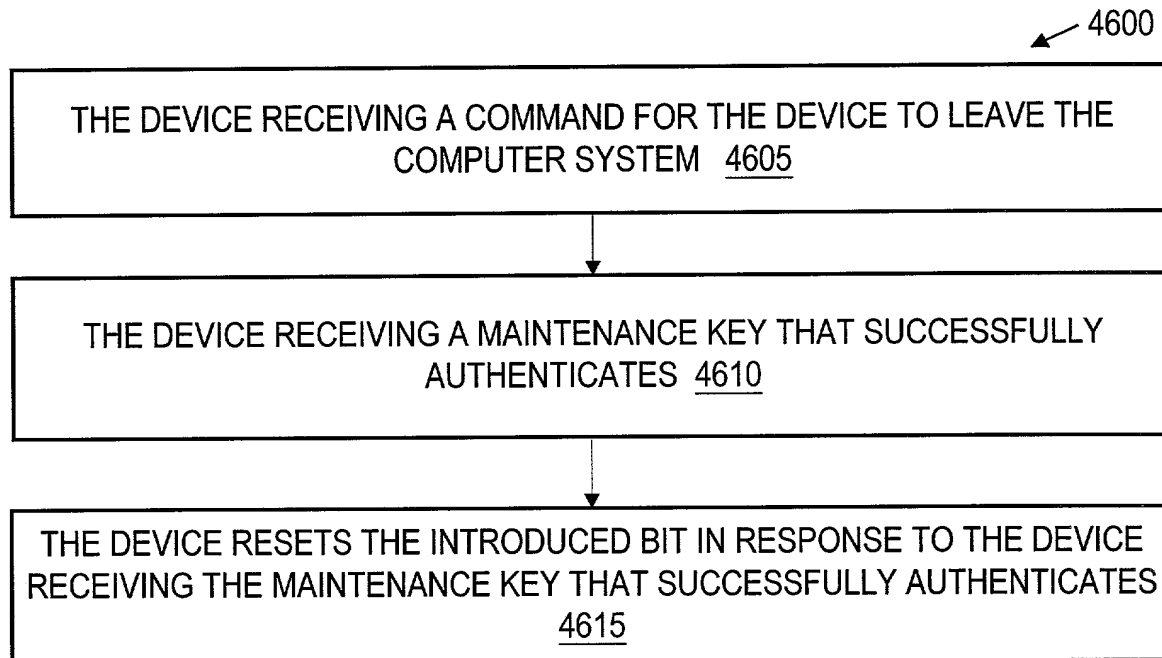


Fig. 35

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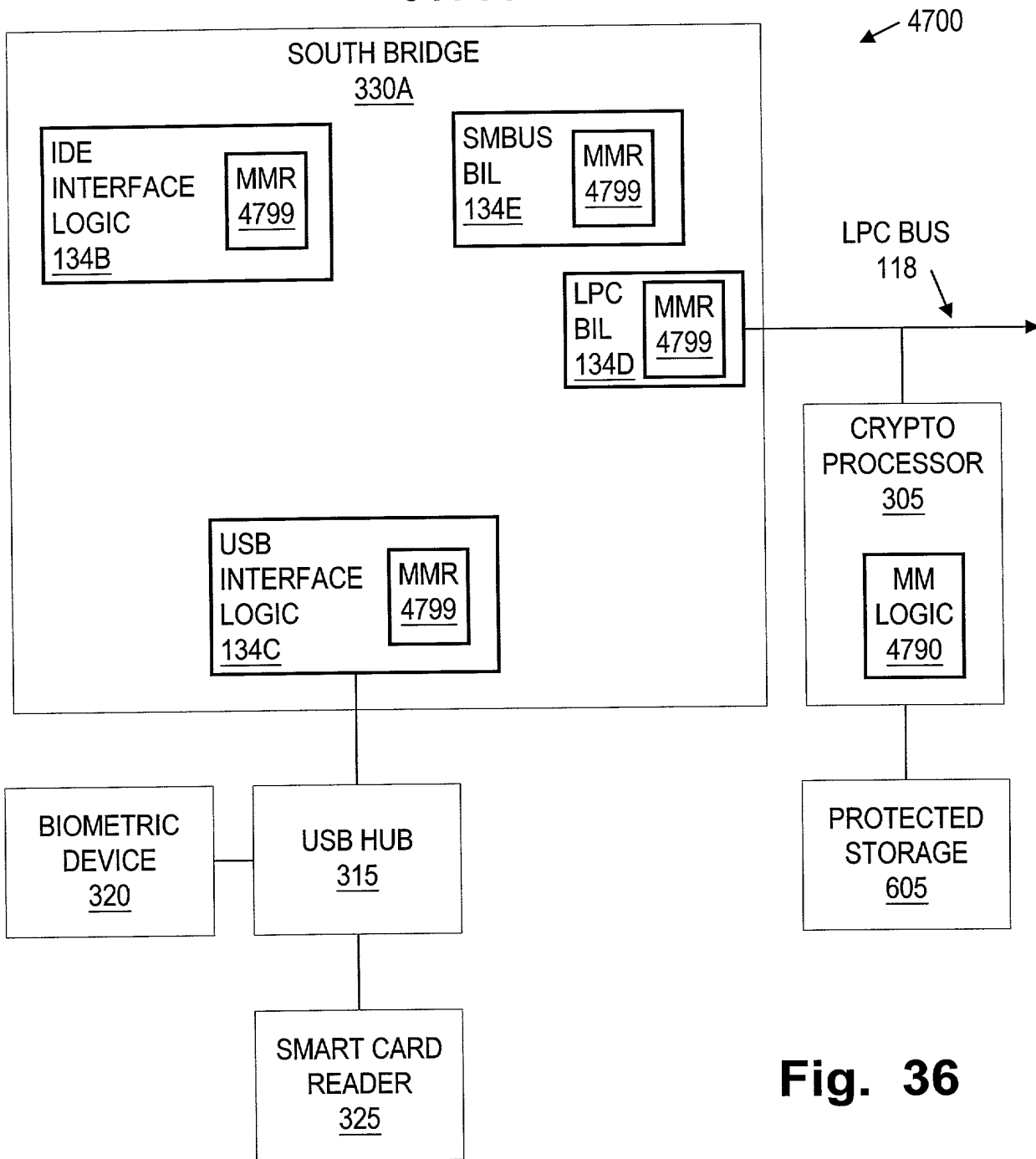


Fig. 36

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4800

TRANSMIT A MASTER MODE SIGNAL TO BUS INTERFACE LOGIC CONNECTED BETWEEN MASTER MODE LOGIC AND A DATA INPUT DEVICE, WHERE THE BUS INTERFACE LOGIC INCLUDES A MASTER MODE REGISTER

4805

SET A MASTER MODE BIT IN THE MASTER MODE REGISTER(S) TO ESTABLISH SECURE TRANSMISSION CHANNEL BETWEEN THE MASTER MODE LOGIC AND THE DATA INPUT DEVICE OUTSIDE THE OPERATING SYSTEM OF THE COMPUTER SYSTEM 4810

THE MASTER MODE LOGIC AND THE DATA INPUT DEVICE EXCHANGE DATA OUTSIDE THE OPERATING SYSTEM OF THE COMPUTER SYSTEM THROUGH THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER 4815

THE MASTER MODE LOGIC FLUSHES THE BUFFERS OF THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER AFTER CONCLUDING THE DATA TRANSMISSIONS 4820

THE MASTER MODE LOGIC SIGNALS THE BUS INTERFACE LOGIC(S) TO UNSET THE MASTER MODE BITS AFTER FLUSHING THE BUFFERS OF THE BUS INTERFACE LOGIC(S) THAT INCLUDE THE MASTER MODE REGISTER

4825

Fig. 37

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4900A

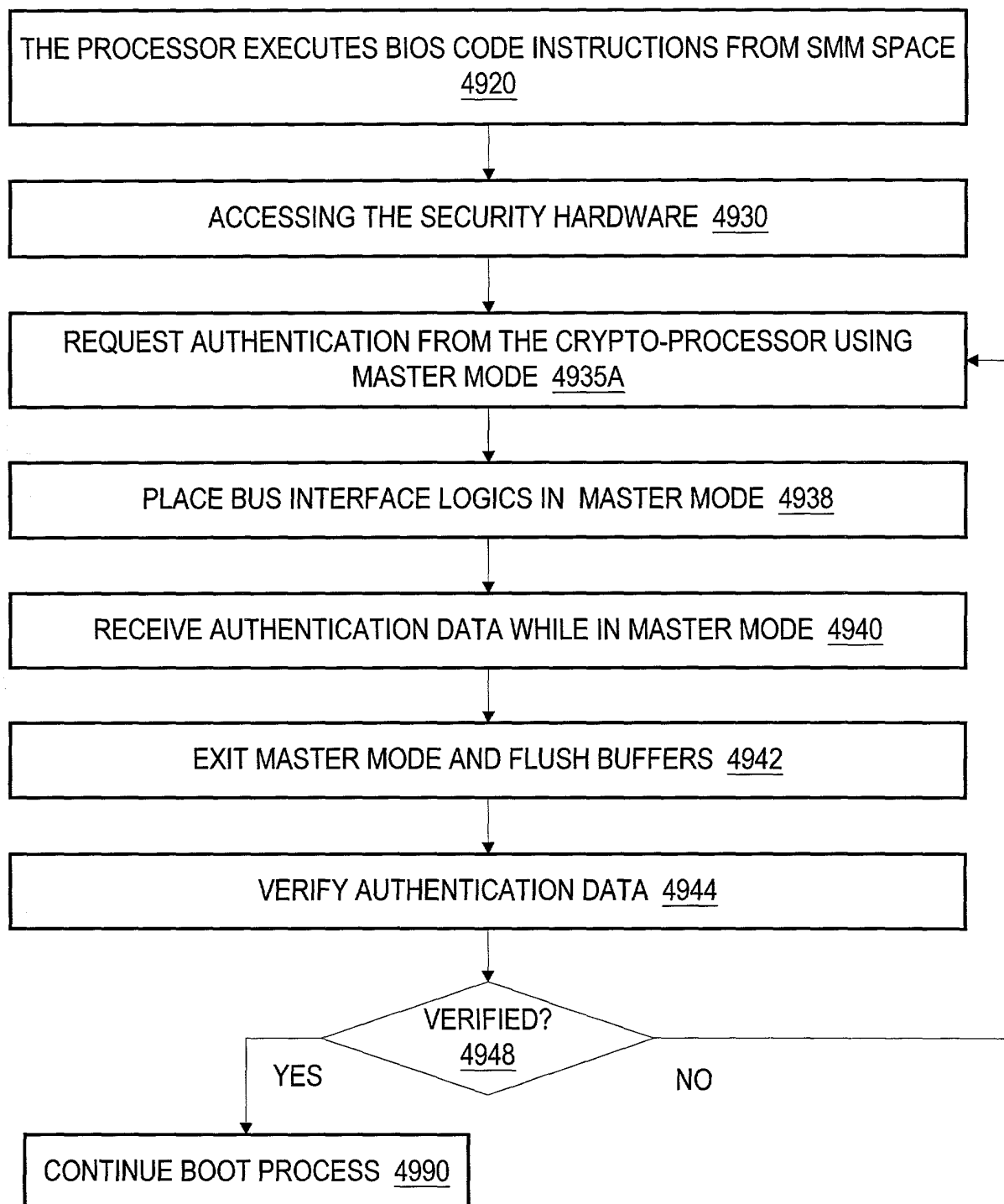


Fig. 38A

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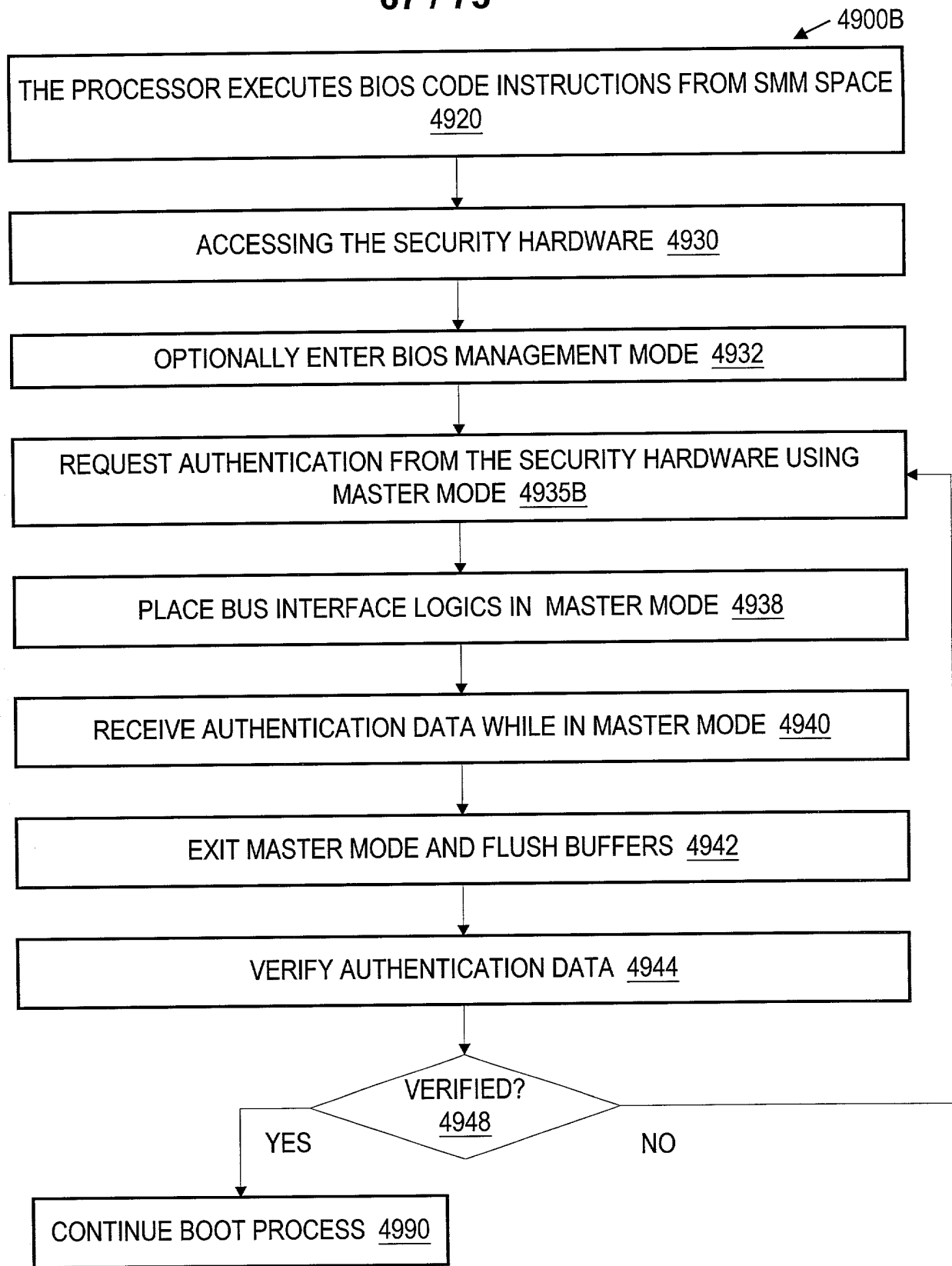


Fig. 38B

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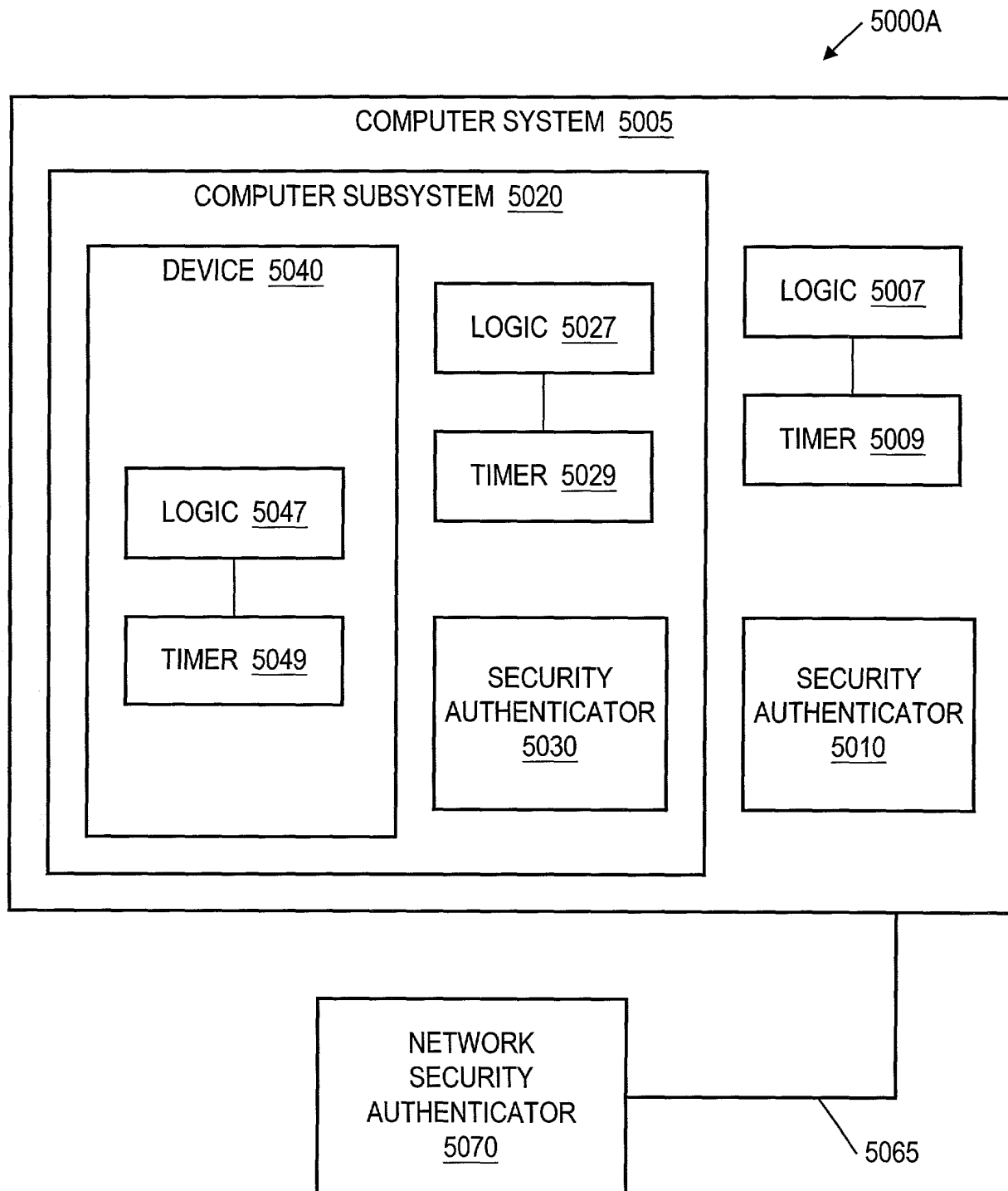


Fig. 39A

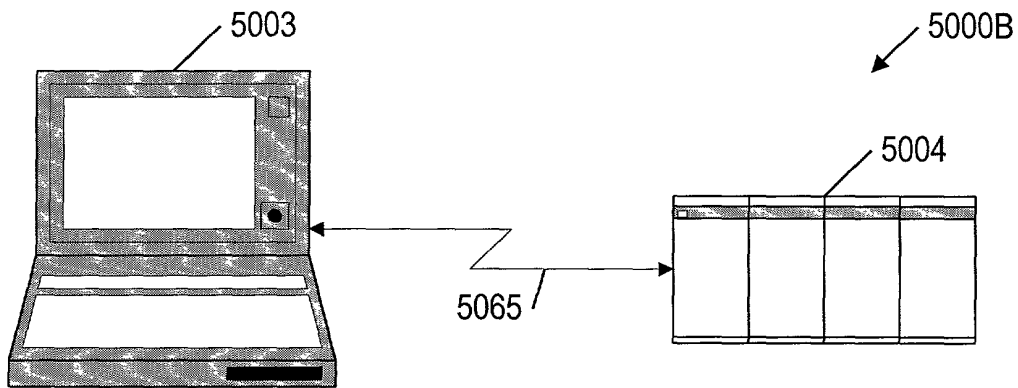


Fig. 39B

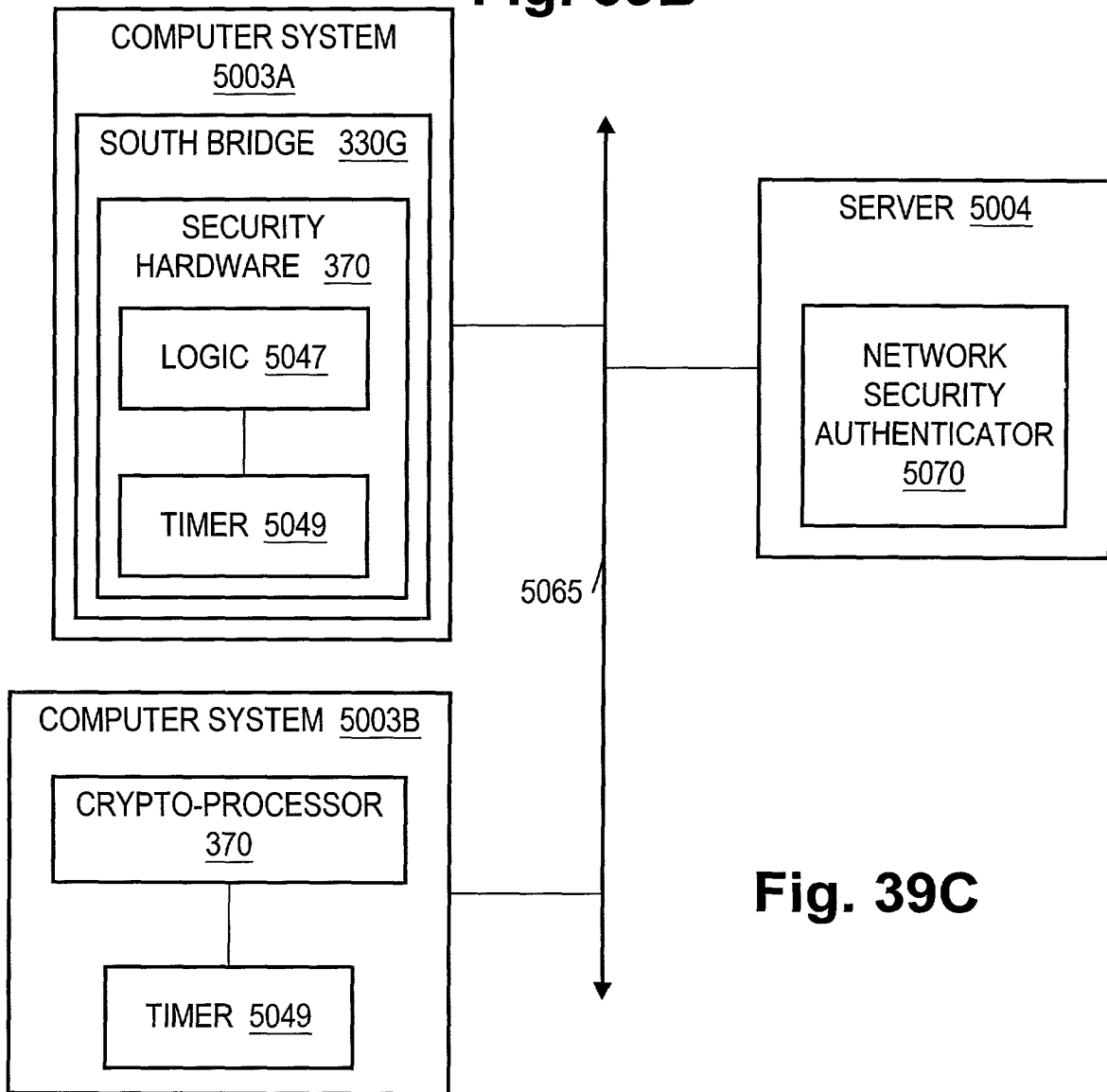
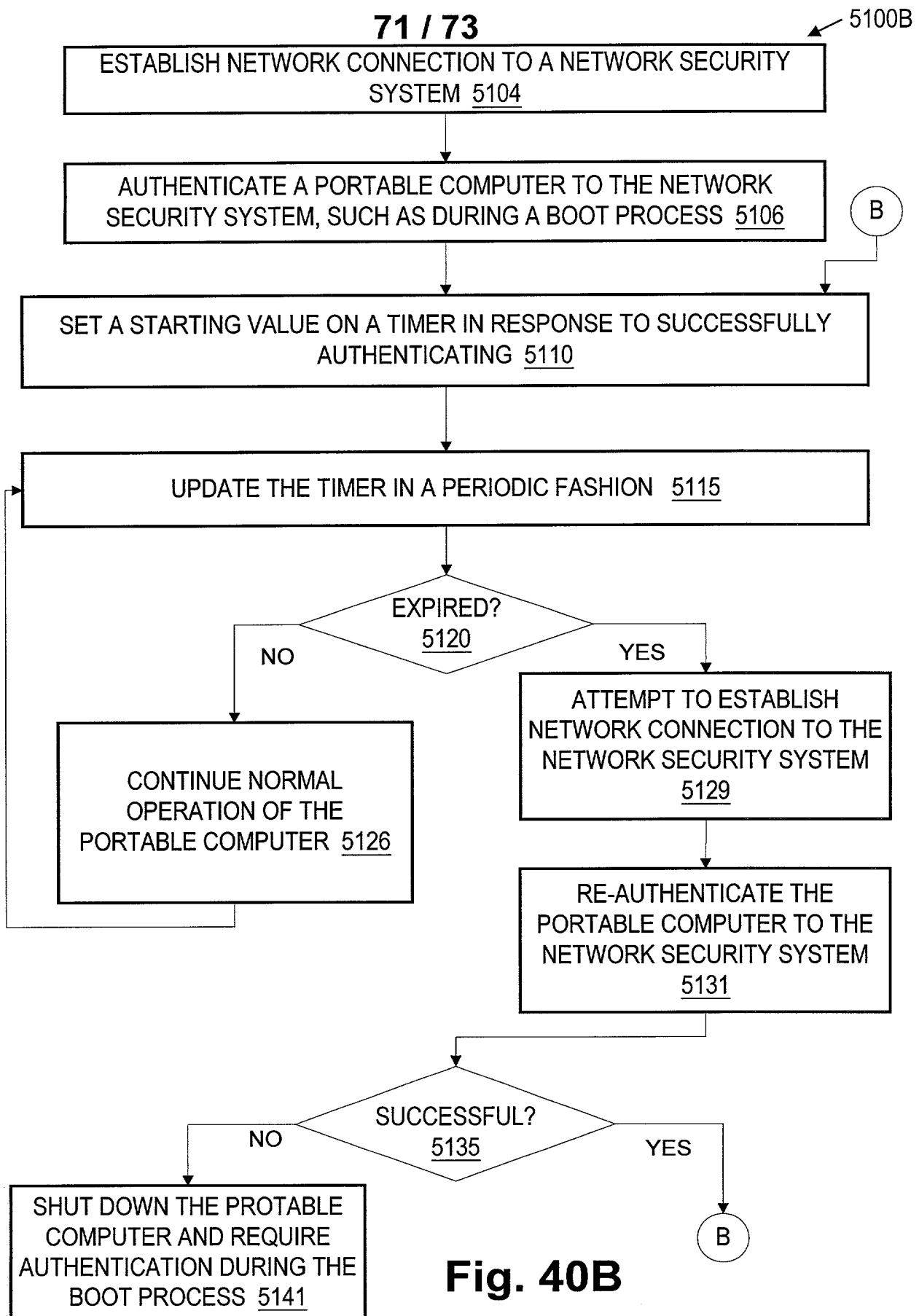


Fig. 39C

5100A





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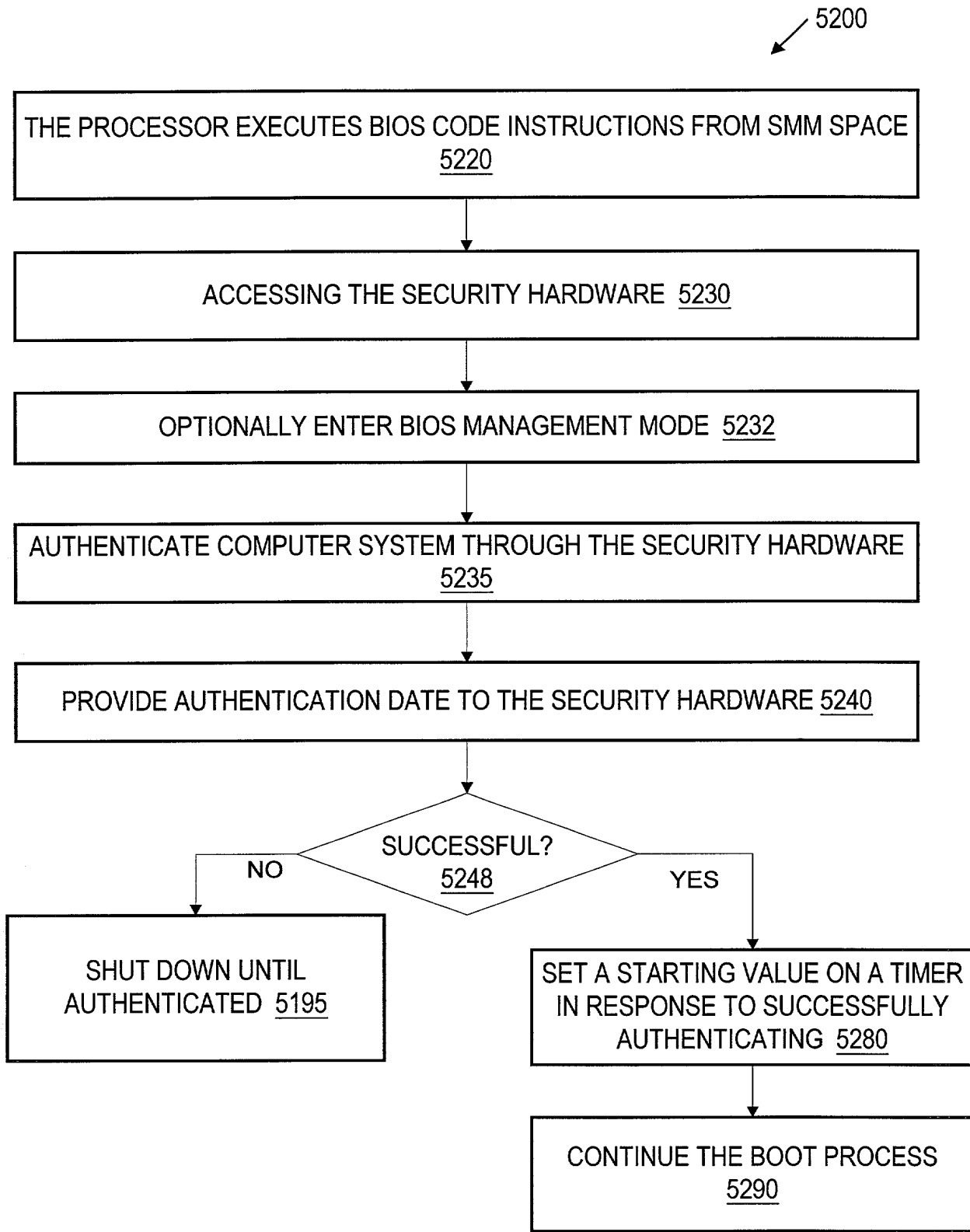


Fig. 41

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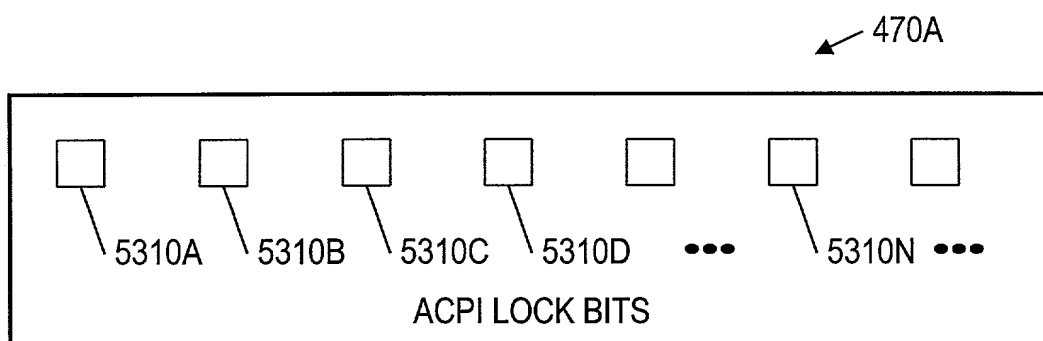


Fig. 42A

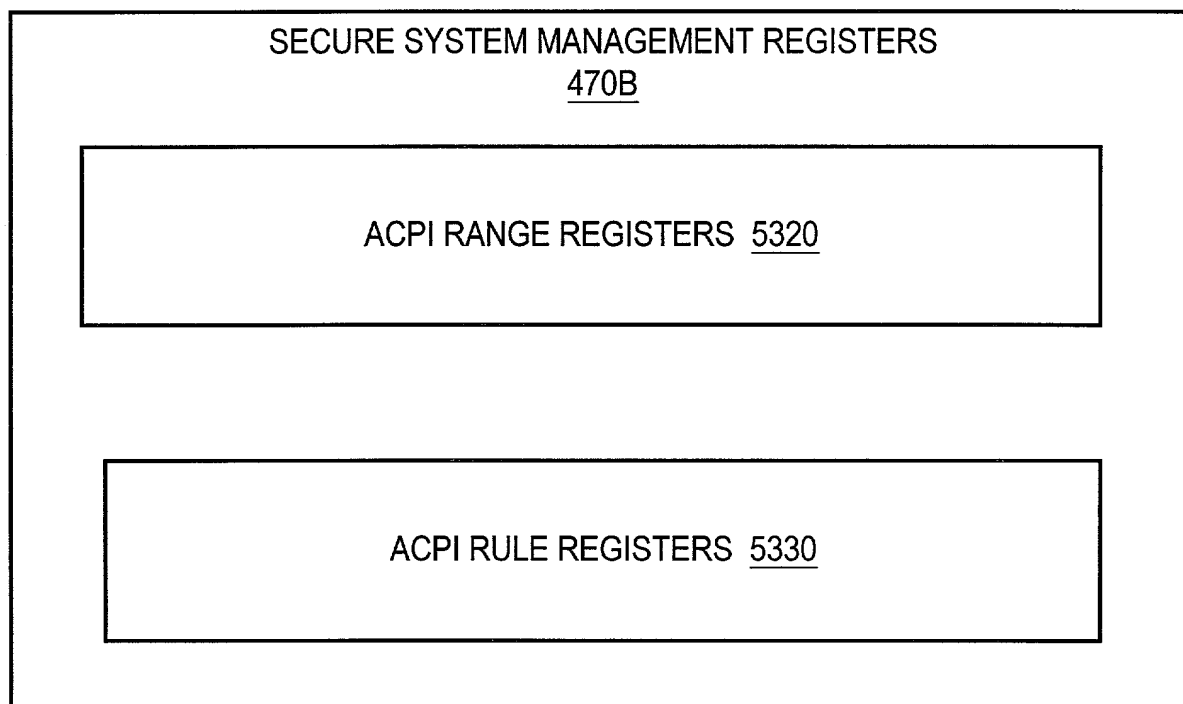


Fig. 42B